



Design Tips

Bruce Archambeault, Associate Editor

Welcome to Design Tips! In this issue, Colin Brench from HP gives us a discussion on EMC Considerations for Differential Lines and Cables. Very high speed signals now use so-called differential signaling to improve signal integrity over long, lossy transmission lines and cables. The impact of these high speed signals on EMC performance can be significant. Colin is well known through the IEEE/EMC Society as a previous Distinguished lecturer, co-author of the book titled 'EMI/EMC Computational Modeling Handbook', and for his many technical presentations, papers, and seminars.

Please send me your most useful design tip for considera-

tion in this section. Ideas should not be limited by anything other than your imagination! Please send these submissions to bruce.arch@ieee.org. I'll look forward to receiving many "Design Tips!" Please also let me know if you have any comments or suggestions for this section, or comments on the Design Tips articles.

Also in this issue, we will be adding "Design Tid-Bits" at the end of the Design Tips Article. These Tid-Bits are intended to be a very short description of EMC design best practices and cover a wide range of EMC design issues. Please send me your contributions to bruce.arch@ieee.org.

Design Tip – EMC Considerations for Differential (Balanced) Lines

Colin Brench

There has been a rapid growth in the use of differential signaling on pairs of conductors for high speed links. A differential line is usually used synonymously with a balanced line; however, there are some serious differences between a fully balanced line and one that is simply used differentially. There are also a number of practical implementation effects that must be carefully considered. These can have a major impact on EMC performance.

First, we should consider the reason for using differential signaling. Over the years, signaling voltage levels have dropped from 12V or so down to one volt or less, and this has come with an increasing sensitivity to noise. The effects of DC or low frequency offsets, that can occur between the transmit and the receive points, are greatly reduced by the common mode rejection of a differential receiver. For EMC, a primary purpose is to cancel the fields created by the current on one conductor with the return current in the adjacent one. This minimizes radiation and reduces the susceptibility to external fields, and so can eliminate the need for an external shield.

A fully balanced scheme requires no separate 'ground' return; it is a two wire system. In reality, not only is a separate ground return not required, it is not wanted; the presence of any closely coupled conductors to a differential pair is a complicating factor that in many cases will result in the generation of unwanted, common mode current. Some interfaces, such as those for Ethernet, use only two wires and are balanced through the use of a transformer or BALUN (balanced to unbalanced network). Unfortunately, in many cases the physical implementations of many differential links are not simple, two wire systems, but rather are comprised of two, independent, single ended circuits. Certainly these circuits switch in opposite polarities, but primarily they are not a balanced differential signaling scheme.

To evaluate any EMC risk that may be present, it is essential to understand all the current paths associated with the signal

path. Initially the device that drives the link typically does so with respect to the reference plane of the printed circuit board; that is, a pair of signal ended signals is generated (see Figure 1). To further understand the signal and return current, consider the PC traces used to connect the driver to an interface connector as shown in Figure 2. From even a casual glance at the trace geometry it can be seen that there is much tighter coupling between the signals and the reference plane than between the two signals.

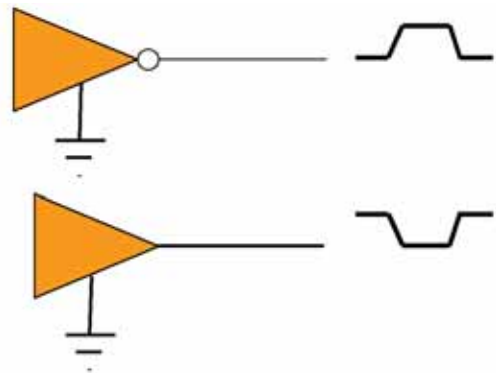


Figure 1--Schematic of a typical differential driver

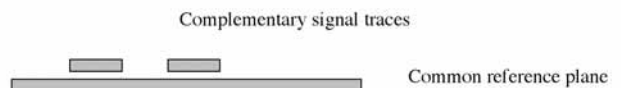


Figure 2--Cross section of PC trace

At the point where the differential signal transitions from the reference plane to a cable, there is a discontinuity in any portion of signaling current that is not perfectly mirrored in the pair of conductors. For the currents to be equal and opposite, as needed for balance, the following features must exist:

1. the amplitude in both circuits must be identical



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2. the load impedance must be identical
3. there can be no skew between rising and falling edges
4. the rise and fall time must be identical
5. the physical trace routes must be not only equal in length overall, but also balanced along their entire length. (End compensation corrects the delay for signal quality but can allow a small imbalance along the conductor length.)
6. coupling to any other conductors must be equal

If the amplitudes of the two signals are not equal, there will be a common mode current in the reference plane having the same frequency content as the intended signal. Figure 3 shows the common mode current generated due to skew between the two lines, and this current will contain frequencies that are higher than the base data.

In a shielded differential pair, there is coupling between each conductor and the shield; the inside of this shield becomes the third conductor that carries any common mode current due to imbalance in the pair. (Unfortunately it will also introduce some imbalance into the pair!) It is therefore necessary to treat a shielded pair as a three wire system and provide a low impedance path from the driver to the receiver, across the PC board and through the cable. Failure to do this will cause a discontinuity in the current path and result in the possibility of excess radiated emissions. This is shown in Figure 4.

In many cases there is an overall EMI shield used to minimize susceptibility to ESD or to further minimize radiated emissions. For this shield to meet its intended function, it must be well bonded to the system chassis so that external EMI is not introduced into the system. This shield should not be carrying any component of the intended signal. However, a path for any current leakage through the shield of the differential pairs to the inside of the overall EMI shield must be provided.

Attention to the details of all paths of the intended differential signaling current and the unintended common mode current is a fundamental way to control EMI and minimize noise

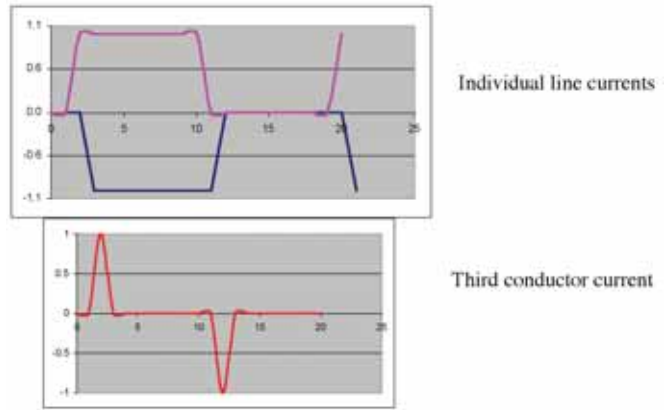


Figure 3--Effect of skew on third conductor current



Figure 4--Connecting a three wire differential line

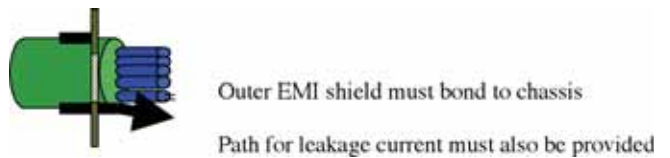


Figure 5--Connection of the EMI shield

coupling into the link. These paths do not happen by accident; in a circuit diagram, 'ground' is 'ground' everywhere, and there is no physical information present. It is, therefore, necessary to consider the physical implementation of the circuit to ensure it performs as expected. **EMC**

Design Tid-Bit

Small amounts of in-pair skew as well as small amounts of rise/fall time mismatch in differential signals are unavoidable. These small amounts of imbalance can create common-mode noise that is close to the same amplitude as the differential signal itself! Consider differential signals to be single ended for EMC purposes and design an unbroken return current path for the common-mode signals. — Bruce Archambeault