



Practical Papers, Articles and Application Notes

Flavio Canavero, Technical Editor

This issue is dedicated to two educational papers, covering two different topics and with two different approaches.

We start with the second contribution of a series of two on the “Meaning of Inductance” by Professor Clayton R. Paul. The first part appeared in the Fall 2007 issue and discussed the topic of loop inductance. This second part deals with partial inductance, and it is a very enlightening contribution on how to attribute and compute inductances to segments of a closed current loop. This concept is crucial for the understanding of signal integrity phenomena like ground bounce and represents valid help for the designers of electronic systems.

The second article is entitled “Effectiveness of PCB Simulation in Teaching High-Speed Digital Design” by Jianjian Song, Keith E. Hoover and Edward Wheeler and is reprinted from the proceedings of the 2007 IEEE International Symposium on EMC held last July in Hawaii. This paper reports on the experience the authors carried out at the Rose-

Hulman Institute of Technology where they introduced simulation tools in undergraduate courses in high-speed design. They argue that the use of a simulation tool in a high-speed digital design class “helps students understand fundamental concepts and ideas in signal integrity as well as to experiment with different techniques for maintaining signal integrity in a PCB design,” and represents “an economical alternative to hardware-based experiments.” I selected this paper in order to stimulate the discussion on new education paradigms.

As always, I encourage all readers to actively participate in this column, either by submitting manuscripts they deem appropriate, or by suggesting other authors having something exciting to share with our EMC community. I will follow up on all suggestions, and with the help of independent reviewers, I hope to be able to provide a great variety of enjoyable and instructive papers. Please communicate with me, preferably by email at canavero@ieee.org.

What Do We Mean By “Inductance”? Part II: Partial Inductance

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Abstract—The concept and calculation of inductance of a current-carrying closed loop were discussed in Part I. In this part we will discuss how to uniquely attribute inductances to segments of a current loop using the concept of partial inductances. The intent of these articles is to provide meaningful and unambiguous formulations of inductance and partial inductance that are based on scientific principles in order to dispel the various misconceptions and erroneous conclusions that have arisen about these important concepts.

Index Terms—inductance, current loops, partial inductance, magnetic flux, Faraday’s law
First we summarize the concept of the inductance of a closed loop of current that was obtained in Part I. Then we will examine the meaning and formulation of partial inductances of that current loop.

I. INDUCTANCE OF CURRENT LOOPS

In Part I, we examined the concept and calculation of the inductance of a loop of current I that encloses a surface s as illustrated in Figure 1. A current produces a magnetic flux density vector \vec{B} about it having units of Webers/m^2 or Tesla. The direction of this

magnetic field is determined by the *right-hand rule*. That is, if we place the thumb of our right hand in the direction of the current, the fingers will point in the direction of the magnetic field that forms concentric circles about the current. Hence this current produces a magnetic flux through the enclosed surface that is directed upwards through that surface if the current is circulating in the counterclockwise direction as in Figure 1. The total magnetic flux ψ due to this current that penetrates the surface s (upward through it) is obtained with a *surface integral* as

$$\psi = \int_s \vec{B} \cdot \vec{ds} \quad \text{Webers} \quad (1)$$

A vector differential surface of that surface is $\vec{ds} = ds \vec{a}_n$ and \vec{a}_n is the unit normal to the surface pointing in the upward direction. The *dot product* $\vec{B} \cdot \vec{ds}$ in the surface integral in (1) means that we take the product of the differential surfaces ds and the components of \vec{B} that are *perpendicular to the surface*. Then we add (with an integral) these products to give the *net magnetic flux ψ leaving (or passing through) the surface s* . This is a sensible result because \vec{B} has two components: one perpendicular to the surface and one that is tangent to the surface. The component of \vec{B} that is tangent to the surface does not contribute to the net flux pass-

ing through the surface.

In order to be able to talk about an inductance of the loop we will assume that the dimensions of the loop are electrically small, i.e., much less than a wavelength. In addition we will assume that the loop perimeter is constructed of a conducting material such as a wire.

The inductance of a current-carrying loop is defined as the ratio of the total magnetic flux penetrating the surface of the loop and the current of the loop that produced it:

$$L = \frac{\psi}{I} \quad \text{Henrys} \quad (2)$$

The magnetic flux ψ through the loop in (1) is directly proportional to the current I that produced it. Hence the inductance L of the loop is only a function of the loop shape and the material properties of the surrounding medium.

According to Faraday's law, the effect of this magnetic field can be represented as a voltage source inserted in the loop as shown in Figure 1. This source has a value that is the rate-of-change of the total magnetic flux penetrating the loop surface:

$$V = \frac{d\psi}{dt} \quad (3)$$

This voltage source can be placed anywhere in the loop: its position in the loop cannot be uniquely determined. The polarity of this induced voltage source in relation to the original current and associated magnetic field is such that it tends to produce an induced current I^{ind} in the loop perimeter that circulates in the clockwise direction (out of its positive terminal). This induced current circulating in the clockwise direction around the loop produces, by the right-hand rule, an induced magnetic field B^{ind} directed downward through the loop surface that opposes (the rate-of-change of) the original magnetic field B that was due to the original current I . Substituting (2) into (3) gives

$$V = L \frac{dI}{dt} \quad (4)$$

which is the usual result for the voltage across the terminals of an inductor. Hence the induced voltage source (that contains the effect of the original magnetic field) can be replaced with the usual inductor symbol as shown in Figure 1, and the voltage developed across it appears at the loop input terminals like a Thevenin open-circuit voltage. It is important to note that *this inductance can be placed anywhere in the loop*: its location *cannot* be uniquely determined.

II. PARTIAL INDUCTANCE OF LOOPS

The question we want to address in this part is "Can we *uniquely* attribute inductances to segments of a *closed current loop*?" The answer to this question is yes! The key to doing so is the concept of *partial inductances* described by Ruehli and Grover [1], [2] and summarized in [3]. Extensive experimental confirmation of the concept of partial inductance was performed by the author and is reported in [4]. Ruehli pioneered the Partial Element Equivalent Circuit or PEEC method of decomposing electromagnetic structures into electric circuit-like models using elements such as partial inductance. The full-wave 3D version of PEEC incorporates the time delays between the fields of one partial element and another partial element. Hence the full-wave version of PEEC is *not* constrained by the requirement that the structure be electrically

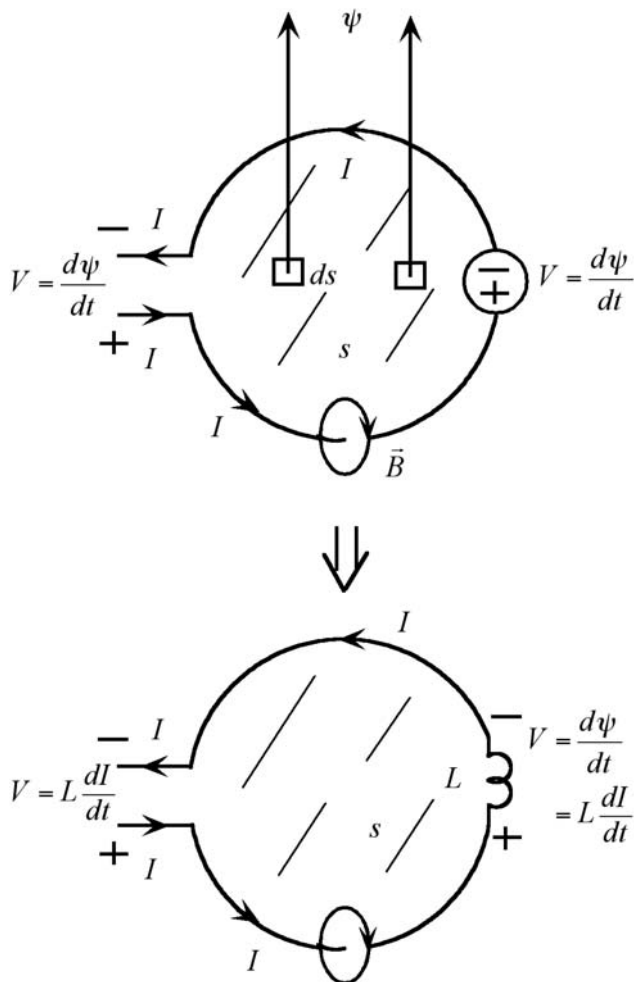


Figure 1.

cally small yet it retains our valuable lumped-circuit analysis insight.

Partial inductance is a perfectly sound concept but has generated skepticism when one does not think in terms of the basic laws and principles on which it is developed. The main problem others have encountered in this discussion of the concept of partial inductance is when they couch the problem in terms of "You can't talk about the inductance of an isolated piece of wire." Of course you can't because inductance is, because of Faraday's law, only associated with a *closed loop of current*. That is not the question. The question is as stated above, "Can we *uniquely* attribute inductances to segments of a *closed current loop*?" The answer to this proper question is yes. Without the concept of the partial inductance of a segment of a conductor, we would not be able to talk about the voltage drop along a section of the conductor that is due to the *rate-of-change of the current through that conductor*, i.e., due to the (partial) inductance of that section of the conductor. A voltage drop along that section that is due to the resistance of that segment of the conductor would only be proportional to the current and not the *time rate-of-change* or derivative of the current.

We often talk about the inductance of a closed loop whether the loop has a current flowing in it or not. In order for the concept of the inductance of a loop to have functional meaning, the loop must be capable of supporting a current, and "an isolated piece of wire" can have no current flowing on it. (An isolated piece of wire in an incident electromagnetic field can have a

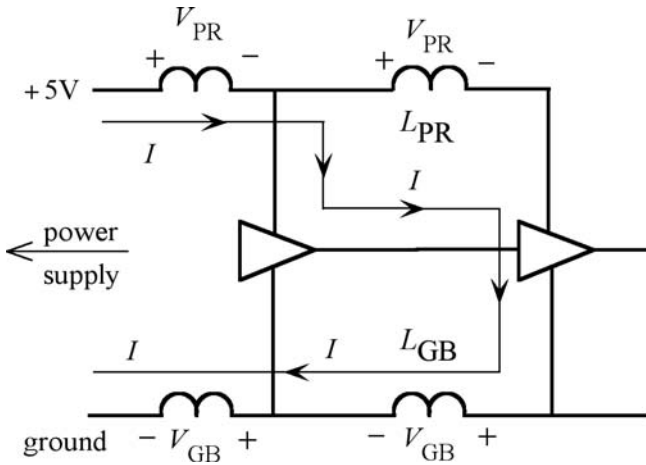


Figure 2.

current induced on it by that field but that is not the same problem.)

One of the important applications of the concept of partial inductance is in the modeling and prediction of “ground bounce” and “power rail collapse” illustrated in Figure 2. Considerable experimental evidence has been obtained [4] showing that when a digital current passes through the return or “ground” conductor and that digital current changes state (“switches”), a voltage will be developed between two points on that return conductor which is proportional to the derivative of that current! Clearly this cannot be due to the resistance of that return conductor or else the voltage drop would be directly proportional to the return current and not its derivative and hence there would be no “ground bounce” of the voltage between two points on the return conductor. This “ground bounce” can cause logic errors in the digital circuitry because the “zero-volt reference” for two modules is no longer the same during this transition of the current between its two states. The magnitude of this ground bounce voltage is proportional to the rate-of-change or slope of the digital current when it changes state. Hence the magnitude of the ground bounce voltage is inversely proportional to the rise/fall times of the current. As the rise/fall times of the digital currents in today’s digital circuitry continues to decrease well into the picosecond range, the magnitudes of the ground bounce voltage are steadily increasing.

The same is true of the +5V power supply connection. When a digital current changes state, the voltage developed across the inductance (partial) of the power supply conductor may cause the voltage of the +5V pin of a module to drop below 5V, which is referred to as “power rail collapse”. This can again lead to logic errors in the digital circuitry. Considerable experimental evidence shows that the voltage between two points on the power supply conductor is proportional to the derivative of the current through it and is not just proportional to the current, as resistance of the conductor would imply. If we accept the fact that ground bounce and power rail collapse are real issues in digital circuit design, we must accept the fact that segments of these conductors in the power distribution loop have inductances that are uniquely attributable to them. Otherwise we would have to say to all digital circuit designers “they need no longer worry about ground bounce and power rail collapse since these don’t exist.”

Similarly, digital circuits employ decoupling capacitors that are

placed close to their modules between their +5V and “ground” pins in order to mitigate the effects of these inductances in producing ground bounce and power rail collapse voltages [3]. During the logic transitions, the current for the module is momentarily drawn from the nearby decoupling capacitor instead of through the long power and “ground” leads from the power supply. During the steady state between transitions of the logic, the decoupling capacitors are slowly recharged by the power supply. We cannot completely eliminate these inductances; we can only minimize their effects through decoupling capacitors or providing closely spaced “going down” and return lands [3]. If partial inductance and the effects resulting from it did not truly exist, we would have no need for decoupling capacitors which no competent EMC engineer would begin removing from their designs. Observe in Figure 2 that the current forms a closed loop from the power supply and returning to it. Hence we may uniquely ascribe partial inductances to the segments of this current loop. A conductor segment can be (and usually is) part of many different current loops. This does not change the fact that the partial inductance of that segment has a unique value independent of the loop(s) that it is a part of, as we will show.

III. DEFINING AND CALCULATING PARTIAL INDUCTANCE

In order to quantitatively define partial inductance we must use two important vector calculus results. First, the divergence of the curl of any vector field is identically zero [5]:

$$\nabla \cdot \nabla \times \vec{A} = 0 \quad (5)$$

This is a sensible result because the curl of a vector field gives its “circulation” or rotation, whereas the divergence gives the field lines “leaving a point”. Next, Stokes’ theorem provides that certain surface integrals may be interchanged with a line integral as [5]

$$\int_S (\nabla \times \vec{A}) \cdot d\vec{s} = \oint_C \vec{A} \cdot d\vec{l} \quad (6)$$

which provides that the surface integral of the curl of a vector field through a surface s is equivalent to the line integral of that vector field around the closed contour c that encircles this surface. The line integral $\oint_C \vec{A} \cdot d\vec{l}$ on the right-hand side of (6) requires that we sum (with an integral) the products of the differential path lengths dl and the components of \vec{A} that are tangent to the path.

Gauss’ law for the magnetic field provides that all magnetic field lines must form closed loops. Mathematically, Gauss’ law for the magnetic field provides that the divergence of the magnetic flux density vector is zero because there are no isolated sources or sinks for the magnetic fields to “diverge to or from” unlike the electric field where electric field lines can begin and end on charge [5]:

$$\nabla \cdot \vec{B} = 0 \quad (7)$$

Because of the vector identity in (5) and Gauss’ law in (7) we are free to define the magnetic flux density vector \vec{B} in terms of an auxiliary variable called the vector magnetic potential \vec{A} as [5]

$$\vec{B} = \nabla \times \vec{A} \quad (8)$$

The vector magnetic potential \vec{A} at all points around a current-carrying wire can be shown to be *parallel to the wire* going to zero at infinity [5]. In addition, *the vector magnetic potential is directly proportional to the current that produced it* [5]. Substituting (8) into Stokes' theorem given in (6) gives the important result:

$$\int_s \vec{B} \cdot \vec{ds} = \oint_c \vec{A} \cdot \vec{dl} \quad (9)$$

Hence *the magnetic flux through a surface s can be alternatively obtained as the line integral of the vector magnetic potential around the closed loop contour c that encloses the surface.*

Substituting the important result in (9) into the basic definition of the inductance of a closed loop gives

$$\begin{aligned} L &= \frac{\psi}{I} \\ &= \frac{\int_s \vec{B} \cdot \vec{ds}}{I} \\ &= \frac{\oint_c \vec{A} \cdot \vec{dl}}{I} \end{aligned} \quad (10)$$

where c is the contour surrounding the surface s for which inductance is defined originally. This result in (10) provides that *the magnetic flux through the surface of a closed loop and hence the inductance of that closed loop can be obtained by adding (with an integral) the products of the components of the vector magnetic potential \vec{A} that are tangent to the contour and the differential lengths of the contour around that closed contour.* This result implies that we may uniquely attribute inductances to segments of the loop contour by expanding (10) as

$$L = \underbrace{\frac{\int_{c_1} \vec{A} \cdot \vec{dl}}{I}}_{L_1} + \underbrace{\frac{\int_{c_2} \vec{A} \cdot \vec{dl}}{I}}_{L_2} + \dots + \underbrace{\frac{\int_{c_n} \vec{A} \cdot \vec{dl}}{I}}_{L_n} \quad (11)$$

where we divide the *closed loop* contour into n segments $c = c_1 + c_2 + \dots + c_n$. This then gives meaning to the assertion above that *we can uniquely attribute inductances to segments of the closed loop contour.*

So we are able to uniquely define the *self partial inductance of a segment c_i of a closed current loop as the ratio of the line integral of \vec{A} along the segment c_i and the current on that segment (which is the current of the loop) as*

$$L_i = \frac{\int_{c_i} \vec{A} \cdot \vec{dl}}{I} \quad (12)$$

Note that the current I of the loop that flows in this segment produces the vector magnetic potential \vec{A} that is to be integrated along the segment, and *this vector magnetic potential is directly proportional to that current* [5]. Hence even if this segment is a part of several different current loops (as it usually is), the value of the self partial inductance of the segment in (12) that is ascribed to this segment is *unique to that segment* and is independent of the loop(s) that the segment is a part of.

Next we provide an understanding of the physical meaning of

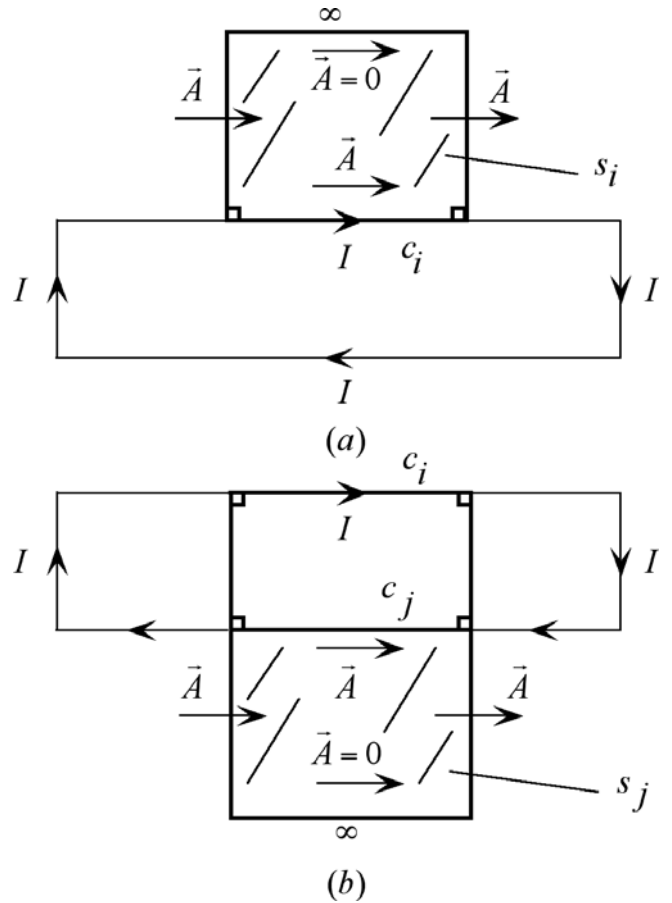


Figure 3.

this partial inductance. Consider a closed, rectangular loop of current I as illustrated in Figure 3(a). Select a segment of this current loop c_i and draw two vertical lines perpendicular to this segment that extend to infinity. These two vertical lines enclose another loop surrounding the surface s_i between the segment and infinity. *If we integrate the line integral of the vector magnetic potential \vec{A} around the surface perimeter enclosed by these lines, we will obtain the total magnetic flux penetrating the loop enclosed by these lines between the conductor segment and infinity.* This is because we may relate the flux through the loop enclosed by these lines to the line integral of \vec{A} around the contour of that loop using (9) to give

$$\begin{aligned} L_i &= \frac{\int_{S_i} \vec{B} \cdot \vec{ds}}{I} \\ &= \frac{\oint_c \vec{A} \cdot \vec{dl}}{I} \\ &= \frac{\int_{c_i} \vec{A} \cdot \vec{dl}}{I} + \frac{\int_{\text{left side}} \vec{A} \cdot \vec{dl}}{I} + \frac{\int_{\text{right side}} \vec{A} \cdot \vec{dl}}{I} + \frac{\int_{\infty} \vec{A} \cdot \vec{dl}}{I} \\ &= \frac{\int_{c_i} \vec{A} \cdot \vec{dl}}{I} \end{aligned} \quad (13)$$

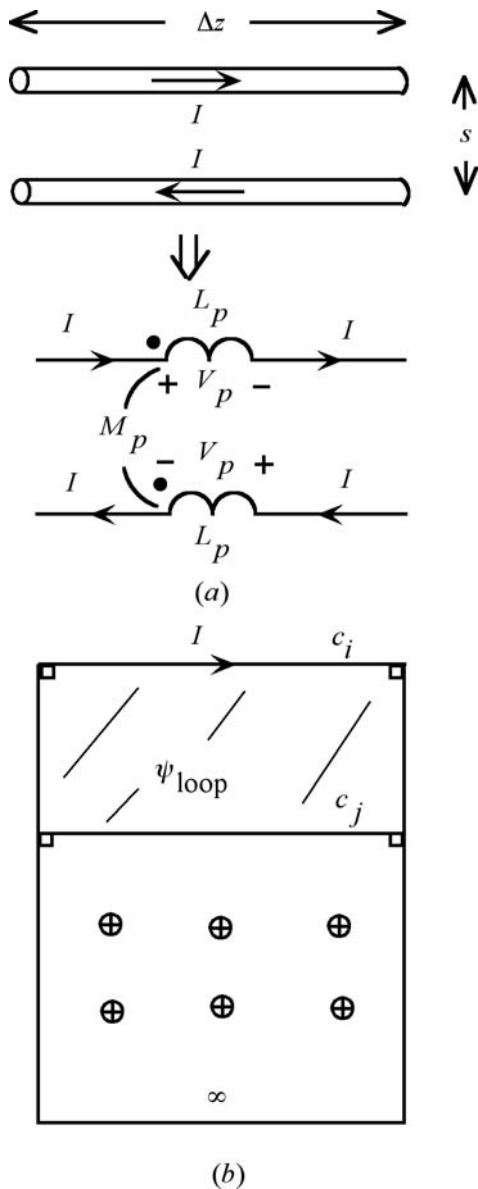


Figure 4.

The result in (13) is due to the fact that the vector magnetic potential along the left and right sides are parallel to the current and hence are perpendicular to the sides. Therefore they do not contribute to the line integral. Similarly, the vector magnetic potential along the top that is at infinity is zero [5] giving the result for the partial inductance of the segment. Hence the important result is:

The self partial inductance of a segment of the contour of a closed loop is the ratio of the magnetic flux penetrating the surface between that segment and infinity and the current of that segment.

Similarly, we can define and give meaning to the concept of the *mutual partial inductance between two segments of the contour of a closed loop*. Select one segment of a closed loop carrying current I_i and denoted as c_i and another segment denoted as c_j as shown in Figure 3(b).

The mutual partial inductance between the two segments c_i and c_j is

$$M_{ij} = \frac{c_j}{I_i} \int \vec{A} \cdot d\vec{l} \quad (14)$$

Again observe that the current I_i along segment c_i produces the vector magnetic potential \vec{A} that is to be integrated along segment c_j , and *the vector magnetic potential is directly proportional to the current that produced it*. Hence even if these segments are parts of several different current loops (as they usually are), the value of the mutual partial inductance between the two segments in (14) is *unique to those segments* and is independent of the loop(s) they are parts of. Because the vector magnetic potential is parallel to the current, the mutual partial inductance between two segments that are orthogonal to each other is zero.

This mutual partial inductance can again be interpreted in terms of the magnetic flux penetrating a surface. Select a segment c_i of the closed loop carrying current I_i as shown in Figure 3(b) and draw two vertical lines perpendicular to that segment and also perpendicular to *another segment of the loop* c_j . Extend these lines to infinity so that they enclose a surface s_j that lies between segment c_j and infinity. Using the same reasoning that we applied to the self partial inductance, we obtain:

The mutual partial inductance between two segments of one or more closed loops is the ratio of the magnetic flux (produced by the current on the first segment) that penetrates the surface between the second segment and infinity and the current of the first segment.

IV. APPLICATIONS TO TRANSMISSION LINES

Now let us apply these results to a two-wire transmission line consisting of two parallel wires shown in Figure 4(a) and show that *the loop inductance can be obtained as a combination of the partial inductances of and between segments of the loop*. The reverse is not true, i.e., we cannot uniquely divide the loop inductance into its partial inductances a priori except in certain special cases such as a square loop having equal-length sides. The partial inductances must be calculated directly. For the two-wire transmission line we will assume that the wires are infinitely long and are close together (as is the usual situation in a transmission line) so that we may neglect the effects of the end segments (which actually are at infinity where the current completes the loop).

In Part I we calculated the *loop* inductance of a section of the line of length Δz as shown in Figure 4(a) by directly calculating the magnetic flux through the loop enclosed by the two wires. The magnetic flux density of a current I of infinite length at a distance r from that current was obtained in Part I as

$$B = \frac{\mu_0 I}{2\pi r} \quad (15)$$

where $\mu_0 = 4\pi \times 10^{-7}$ is the permeability of the surrounding free space. This magnetic field forms concentric circles about the current with a direction of the field determined by the right-hand rule, i.e., placing the thumb of our right hand in the direction of the current, the fingers give the direction of the resulting magnetic field about the current. In Part I we superimposed the magnetic fluxes (due to the two line currents) through the loop enclosed by the two transmission-line wires using (1) and (15) to give the inductance of the enclosed loop as

$$L_{\text{loop}} = \frac{\mu_0}{\pi} \Delta z \ln \left(\frac{s}{r_w} \right) \quad (16)$$

A section of the line is modeled with partial inductances as shown in Figure 4(a). Grover and Ruehli show that the self and

mutual partial inductances for two parallel straight wires of lengths Δz and separation s (for wires of radii r_w) are [1]–[3]

$$L_p = \frac{\mu_0}{2\pi} \Delta z \left[\ln \left(\frac{2\Delta z}{r_w} \right) - 1 \right] \quad (17a)$$

$$M_p = \frac{\mu_0}{2\pi} \Delta z \left[\ln \left(\frac{\Delta z}{s} + \sqrt{1 + \frac{\Delta z^2}{s^2}} \right) - \sqrt{1 + \frac{s^2}{\Delta z^2}} + \frac{s}{\Delta z} \right]$$

$$\cong \frac{\mu_0}{2\pi} \Delta z \left[\ln \left(\frac{2\Delta z}{s} \right) - 1 \right] \quad \Delta z \gg s \quad (17b)$$

Self and mutual partial inductances for conductors of rectangular cross section (PCB lands) can be calculated using the results in Hoer and Love [6]. From the equivalent circuit in terms of partial inductances in Figure 4(a) we can obtain the inductance of the loop of length Δz . The voltage across each self partial inductance is, using the dot convention for mutual inductance [7], [8],

$$V_p = L_p \frac{dI}{dt} - M_p \frac{dI}{dt}$$

$$= (L_p - M_p) \frac{dI}{dt}$$

$$= \frac{\mu_0}{2\pi} \Delta z \ln \left(\frac{s}{r_w} \right) \frac{dI}{dt} \quad (18)$$

The total voltage drop around the loop is twice the result in (18). Hence the loop inductance is

$$L_{\text{loop}} = 2(L_p - M_p)$$

$$= \frac{\mu_0}{\pi} \Delta z \ln \left(\frac{s}{r_w} \right) \quad (19)$$

which is the loop inductance result obtained directly in Part I.

The result in (19) that the net *loop* inductance for the transmission line segment is related to the difference between the self and mutual partial inductances is a sensible result based on the physical interpretation of partial inductances as being related to the flux through a loop that extends from the segment to infinity. Figure 4(b) shows this reasoning. The self partial inductance of segment c_i is due to the magnetic flux between that segment and infinity, whereas the mutual partial inductance between segments c_i and c_j is due to the magnetic flux produced by the current on segment c_i that penetrates the loop between segment c_j and infinity. The net magnetic flux penetrating the loop between the two transmission-line conductors is the difference of these two magnetic fluxes.

The voltages V_p across the self partial inductances in (18) are the “ground bounce” and “power rail collapse” voltages alluded to earlier. Each partial inductance is the ratio of the magnetic flux between that conductor and infinity and the current that produced it. Hence as we bring the two conductors of the transmission line closer, the mutual partial inductance approaches the

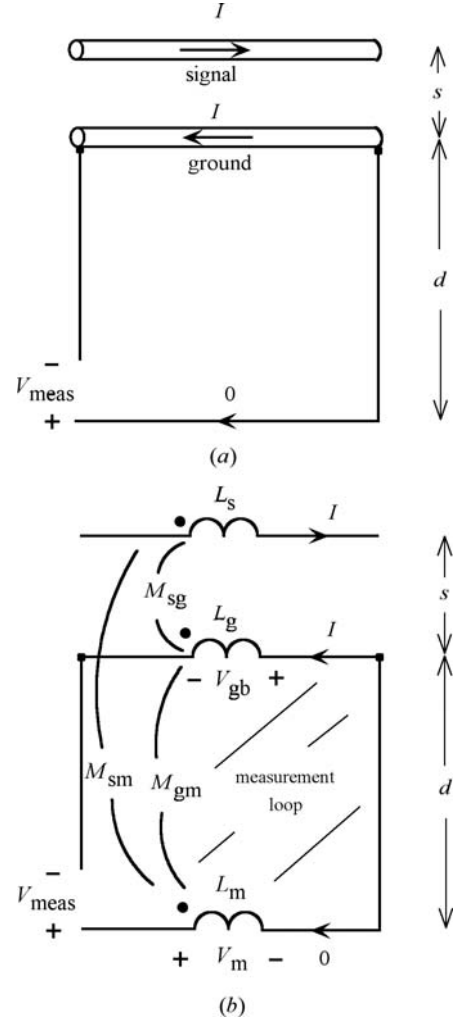


Figure 5.

self partial inductance, $M_p \rightarrow L_p$, and the “ground bounce” and “power rail collapse” voltages approach zero, $V_p \rightarrow 0$, and are minimized. This confirms our earlier assertion that in order to minimize the effects of these partial inductances and the resulting “ground bounce” and “power rail collapse” voltages, we should route the “going down” and return conductors of the transmission line *close together*.

Modeling the transmission line with partial inductances also shows how to *properly measure* the “ground bounce” voltage between the two ends of the return or “ground” conductor of a transmission line [4], [9]. To correctly measure this voltage, we should attach the leads of a voltage measurer (assumed to have a very large input impedance such that it draws no current) to the two ends of the return conductor, place the voltage measurer at a distance d that is *as far away as possible from the transmission line*, and route the leads connecting the two measurement points to the voltage measurer *perpendicular to the conductor* as illustrated in Figure 5(a). Actually the voltage measurer need not be placed very far from the “ground” conductor, i.e., d does not need to be very large, in order to obtain an accurate measurement of the “ground bounce” voltage. Extensive experimental results reported in [4] show that the measured voltage converges rapidly as the voltage measurer is moved further away from the “ground” conductor.

To prove the validity of this measurement scheme, model the line and the measurement leads with partial inductances as shown in Figure 5(b). Because two sections of the connection leads between the conductor and the voltage measurer (which form the sides of the “measurement loop”) are perpendicular to the currents of the transmission line, there are no mutual partial inductances between them and the transmission line conductors. They still have self partial inductances but because there is no current flowing around this measurement loop, the self partial inductances of the sides have no effect on the measured voltage and are therefore not shown in the figure. The only mutual partial inductances are those between the two parallel conductors of the line and the remaining conductor of the measurement loop that is “far away” and also parallel to the transmission line conductors. The measured voltage is

$$V_{\text{meas}} = V_m + V_{\text{gb}} \quad (20)$$

where V_m is the voltage across the self partial inductance L_m of the far-away portion of the connection lead to the voltage measurer (which has no current through it), and V_{gb} is the “ground bounce” voltage *whose value is to be measured*. From the circuit in Figure 5(b) we obtain the “ground bounce” voltage to be measured as before as

$$V_{\text{gb}} = (L_g - M_{\text{sg}}) \frac{dI}{dt} \quad (21)$$

where L_g is the self partial inductance of the “ground” conductor and M_{sg} is the mutual partial inductance between the signal and “ground” conductors of the transmission line. Similarly, the voltage across L_m is

$$V_m = (M_{\text{sm}} - M_{\text{gm}}) \frac{dI}{dt} \quad (22)$$

where M_{sm} is the mutual partial inductance between the signal conductor of the transmission line and L_m , and M_{gm} is the mutual partial inductance between the “ground” conductor of the transmission line and L_m . There is no contribution to the voltage in (22) due to the self partial inductance L_m because the current through it is *zero* since the voltage measurer draws no current through its measurement leads. According to (20), in order for the measured voltage to equal the “ground bounce” voltage, we must have $V_m = 0$. This can only be the case if

$$M_{\text{sm}} = M_{\text{gm}} \quad (23)$$

From (17) we obtain

$$\begin{aligned} (M_{\text{sm}} - M_{\text{gm}}) &= \frac{\mu_0}{2\pi} \Delta z \ln \left(\frac{d}{s+d} \right) \\ &= -\frac{\mu_0}{2\pi} \Delta z \ln \left(\frac{s}{d} + 1 \right) \\ &\cong -\frac{\mu_0}{2\pi} \Delta z \frac{s}{d} \quad d \gg s \end{aligned} \quad (24)$$

If the voltage measurer is placed far away from the transmission line conductors, i.e., d is made very large compared to the transmission line conductor separation s , $(M_{\text{sm}} - M_{\text{gm}}) \rightarrow 0$ and

the measurement voltage is equal to the “ground bounce” voltage.

This proper measurement scheme seems counter intuitive since one might think that we should perhaps route the connection leads to the voltage measurer along and close to the “ground” conductor in order to eliminate the area enclosed by the measurement loop. If the measurement leads were routed close to the “ground” conductor, then $M_{\text{gm}} \rightarrow L_g$ and $M_{\text{sm}} \rightarrow M_{\text{sg}}$, and the measured voltage would approach zero:

$$\begin{aligned} V_{\text{meas}} &\cong \underbrace{(M_{\text{sg}} - L_g) \frac{dI}{dt}}_{V_m} + \underbrace{(L_g - M_{\text{gm}}) \frac{dI}{dt}}_{V_{\text{gb}}} \quad (25) \\ &= 0 \end{aligned}$$

Hence as the measurement leads are brought closer to the “ground” conductor, the measured voltage would approach zero which is clearly not equal to the “ground bounce” voltage (unless you want to say that the “ground bounce” voltage “doesn’t exist”)! This result is easily seen from Figure 5 using Faraday’s law. As the measurement leads are brought closer to the “ground” conductor, the measurement loop area between the “ground” conductor and the measurement lead conductors approaches zero. Hence by Faraday’s law, the emf induced in that loop, which is V_{meas} , approaches zero.

This is an example of where “intuition” that is not based on scientific principles and laws can get us into trouble. The problem here has to do with the fact that in order to measure a voltage between two widely-spaced points we must connect the voltage measurer to those points with *nonzero* lengths of measurement leads. The notion of routing the measurement leads close to the “ground” conductor in order to measure the “ground bounce” voltage between the two ends of the “ground” conductor comes about from our thinking of the measurement leads as having only a resistance and forgetting about them having an inductance and an enclosed area. This is a dc or low frequency way of thinking that we must avoid. Thinking of these measurement leads as only having a resistance is not the complete (or most important) part of the picture. Extensive experimental results given in [4] confirm this result. Skilling gives an alternative argument for the correctness of this scheme in [9].

V. SUMMARY

The purpose of this series of articles is to examine the concept and calculation of inductance using scientific principles in order to dispel popular misconceptions about this important and fundamental concept. In this part we examined how to uniquely attribute inductances to segments of a *closed current loop* using the concept of partial inductance. Partial inductance allows the unambiguous calculation of the voltage drop between two ends of a segment of a closed loop so that we can calculate and understand how to mitigate ground bounce and power rail collapse in order to ensure signal integrity. This is crucial to our ability to design an electronic system to prevent it from “shooting itself in the foot”. The concept of partial inductance provides considerable insight that is crucial to the design of an electronic circuit for signal integrity.

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BIOGRAPHY



Clayton R. Paul (S'61-M'70-SM'79-F'87-LF'06) received the BS degree from The Citadel, Charleston, SC in 1963, the MS degree from Georgia Institute of Technology, Atlanta, GA in 1964, and the PhD degree from Purdue University, Lafayette, IN in 1970, all in electrical engineering.

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Effectiveness of PCB Simulation in Teaching High-Speed Digital Design

Jianjian Song, Keith E. Hoover and Edward Wheeler (song@rose-hulman.edu)

Abstract—Signal integrity for high-speed digital design at the printed-circuit board (PCB) level is an issue of increasing importance in electronic design that requires coverage in more undergraduate classes. This paper describes how simulation tools offer an economical alternative to hardware-based experiments in undergraduate courses in high-speed design. A simulation tool, Hyperlynx, has been used in our high-speed digital design class to help students understand fundamental concepts and ideas in signal integrity as well as to experiment with different techniques for maintaining signal integrity in a PCB design.

We present examples in which traditional approaches employing only closed-form expressions can be effectively supplemented with simulation to help students gain a deeper understanding of basic concepts such as time-of-flight, parasitic parameters, nonlinear driver and receiver models, characteristic impedance, per-unit-length parameters, termination techniques, and crosstalk.

I. INTRODUCTION

Signal integrity in digital electronic systems has become a critical topic in electronic system design at the printed circuit board (PCB) level. At high clock frequencies, maintaining signal integrity becomes both challenging to achieve and important to system reliability. It is well known that signal integrity issues are often directly related to electromagnetic compatibility performance so that a system well designed to maintain the former would also result in a better performance for the later.

Signal integrity has been included in college curricula [1]–[3]. Topics relating to signal integrity at the PCB level often include noise and timing margins, models for drivers and receivers, transmission lines, load termination, crosstalk due to capacitive and inductive coupling, and ground and power noises.

Traditional approaches to high-speed PCB design use a number of closed-form equations for estimating noise margin and timing margin. These expressions, based on simple linear driver and receiver models, are obtained from physical circuits through simplifying assumptions and are excellent in providing design guidelines but cannot be used to predict accurately the behavior of real devices. We feel that simulation tools incorporating accurate and readily available device input and output models such as the I/O Buffer Interface Specification (IBIS) should be incorporated in undergraduate courses on signal integrity at the PCB level. Our experience shows that these tools are a practical and cost-effective addition in teaching signal integrity in high-speed design in undergraduate engineering curricula.

As more accurate input and output buffer models such as I/O Buffer Interface Specification (IBIS) [7] have gained widespread

use and acceptance and PCB simulation tools have become more accurate and affordable, these tools can be important additions to any class in high-speed design. PCB simulation tools, in conjunction with conceptual understanding and closed-form expressions can be used together to help students learn effectively about real world high-speed design practices.

PCB simulation needs to be an integral part of a lab-based undergraduate class on signal integrity, especially when physical experiments of high-speed electronics often prove too costly. A number of companies provide simulation tools for signal integrity at PCB level. Some popular tools are from companies such as Cadence, Sigrity, and Mentor-Graphics [3], [8].

A PCB simulation tool, Hyperlynx from Mentor Graphics has been used in our high-speed digital design class because of its ease of use, its intuitive user interface, and its flexibility for evaluating pre-layout and post-layout designs.

This paper presents our approach and experience in using Hyperlynx. A number of examples of PCB simulation are presented which can be used to help students learn concepts such as time-of-flight, parasitic parameters, driver and receiver models, characteristic impedance, and per-unit-length parameters. Section II describes an example of how clock speed for a digital circuit can be estimated. Section III shows termination technique evaluation with simulation and Section IV provides a crosstalk example.

II. LIMITING FACTORS ON CLOCK SPEED OF A CIRCUIT

Clock speed of a clock-synchronous circuit is limited by a number of factors such as noise margins, timing margins, and rise and fall times. Noise sources include power supply, ground bounce, PCB trace reflection, capacitive or inductive coupling, radiated or conducted coupling and thermal noise. Timing of a clock signal can be affected by device delays, setup and hold times, PCB trace delays and crosstalk. Loading and crosstalk can affect the rise and fall times of a clock signal.

A. Traditional Approach

Traditional approaches to clock speed estimation assume simple linear driver and receiver models. Noise margins are estimated from pullup and pulldown resistors to model “ON” and “OFF” resistances of a driver and from the capacitive load for a receiver. The resistors are in general extracted from eight DC parameters on the data sheet of a device [9]. Although these parameters can be readily obtained and the resistances are easy to calculate, the resulting model does not match the nonlinear behaviour of input and output buffers of a device.

Timing margin is estimated by adding component delays, trace delay or time-of-flight for each path involved, possible crosstalk, and clock jitter [5]–[6]. It is more difficult with this

approach, based solely on closed-form expressions, to include other influences on signal integrity such as ringing, multiple reflection, ground and power bounce.

B. Simulation Approach

PCB simulation tools together with more accurate input and output buffer models can analyze noise margins, timing margin, and rise and fall times so that clock speed limits can be estimated realistically. An example is given in this section to show how easy and effective a simulation tool can be. The PCB simulation tool is Hyperlynx from Mentor Graphics.

The experiment in this section was originated from [8], where compensation time and time-of-flight are calculated with LineSim of Hyperlynx. We expanded the idea to examine how fast the digital circuit from [8] can be clocked. In order to investigate this question, we would need to understand the rise and fall times and noise margins of the device driver and receiver. We would also need to construct a PCB circuit and connect the right IBIS models for the driver and receivers.

C. Understanding Drivers and Receivers with Visual IBIS Editor

Two devices, a 32-bit Microprocessor chip RC32355 and a SRAM chip IDT71V67603 from Integrated Device Technology are used to evaluate signal integrity [8]. Their IBIS files can be obtained from www.idt.com. Visual IBIS Editor from Hyperlynx can evaluate the IBIS files and correct any existing syntax errors. Two specific signal pins, one from each of the two chips are examined: the clock output sysclkp of the RC32355 in Figure 1 and the clock input pin, CLK, of the 71V67603.

All curves in an IBIS model could be checked such as Power and Ground Clamp V-I curves, Pullup and Pulldown V-I curves, and rise and fall slew rates, V-T rise and fall curves from their IBIS models.

Typical rise and fall times, output voltage high minimum, V_{oh} , and output low maximum, V_{ol} , for the clock output sysclkp can be found from its V-T curves. The model for sysclkp pin shows the supply voltage of 3V and the typical logic high voltage is $V_{oh} = 2.72V$. From the V-T rise curve of the pin in Figure 1, it can be seen that it takes typically 1.5866ns to change from 300mv to 2.448v, which is 90% of 2.72V. V_{ol} can be found from the falling waveforms and is 0.7V in the worst case.

The model for the input clock pin CLK of the SRAM also indicates input voltage low maximum V_{inl} is 0.800V and input voltage high minimum V_{inh} is 2.000V. The DC noise margins for the pin are therefore $2.72 - 2 = 0.72V$ for high logic state and $0.8 - 0.3 = 0.5V$ for low logic state when the SRAM is clocked by the controller.

D. Observing and Evaluating Circuit Parameters

A trace layout is replicated from [8] with LineSim of Hyperlynx as shown in Figure 2. Students can use the transmission line geometry and parameter editor to explore options to obtain a trace with fixed length, characteristic impedance, and time-of-flight.

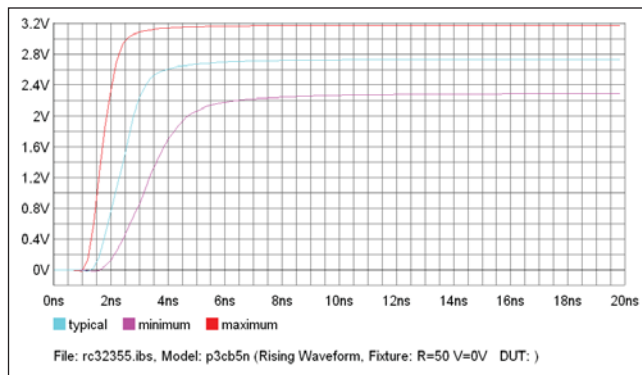


Figure 1. The rising waveforms of driver pin sysclkp of the RC32355.

E. Estimating the Highest Clock Speed for the Circuit

The noise margins for all the driver and receiver pins in Figure 2 are given in Table 1. Three factors that limit how fast the clock can operate are noise margins, rise times, and fall times. The logic high and low voltage levels must be within the required noise margins for the circuit to work reliably. The rise time and fall time of the clock cannot be slower than the required values in order for the circuit to be synchronized correctly.

TABLE I. NOISE MARGINS FROM THE DRIVER TO THE RECEIVERS.

In volts	V_{inH}	V_{inL}	V_{outH}	V_{outL}
RC32355 sysclkp	2.0	0.8	2.8	0.7
71V67603 CLK	2.0	0.8		
Noise Margins			0.8	0.1

Figure 3 shows two example simulations at 150MHz and 200MHz. It can be seen that the circuit works correctly at

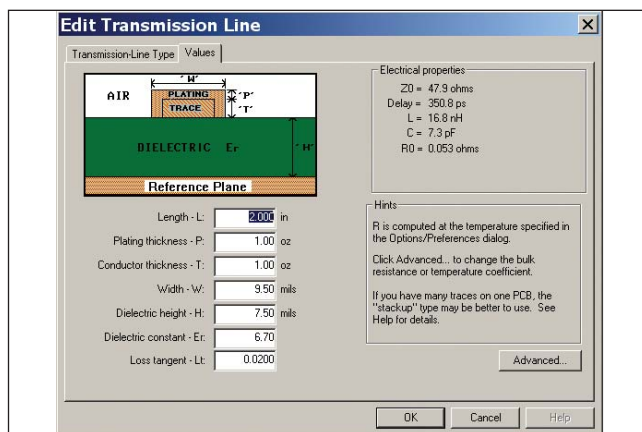
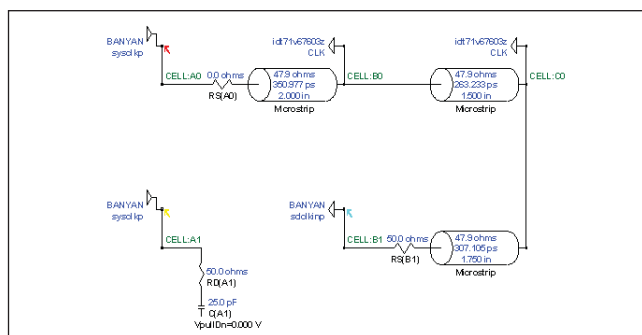


Figure 2. The circuit with one driver and two receivers.

150MHz but not at 200 MHz because the low logic level voltage at 200MHz is above the maximum required.

III. EXPLORING TERMINATION STRATEGIES

A number of termination techniques are introduced in various textbooks and articles. They include series, RC, parallel, Thevenin, and controlled impedance terminations as well as termination for a differential pair [4]–[5], [10]. The goal in termination analysis is to determine resistance values, power dissipation, and effects on noise margins and timing margins. An optimal solution to a termination problem involves compromises among the above factors.

A. Traditional Approach

Traditional approaches to termination analysis provide a number of empirical or theoretical equations based simple linear models for input and output buffers [5], [10]. The analysis cannot be generalized to treat varying load and transmission line characteristics easily.

For example, using a Thevenin termination would involve noise margin analysis [5], [10]. The formula analysis may not match or model an actual circuit well. Another example is source series termination where a series resistor is added to the source resistor of the driver to match the characteristic impedance of a trace connected to the driver output [10]. The source resistor derived from the data sheet for a device may not be accurate over a range of operating conditions of the driver since this resistance is a nonlinear function of operating conditions.

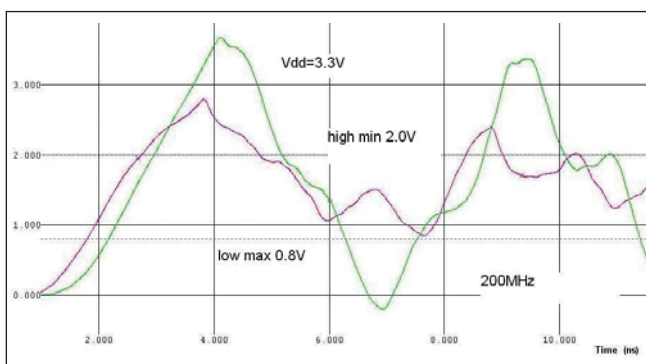
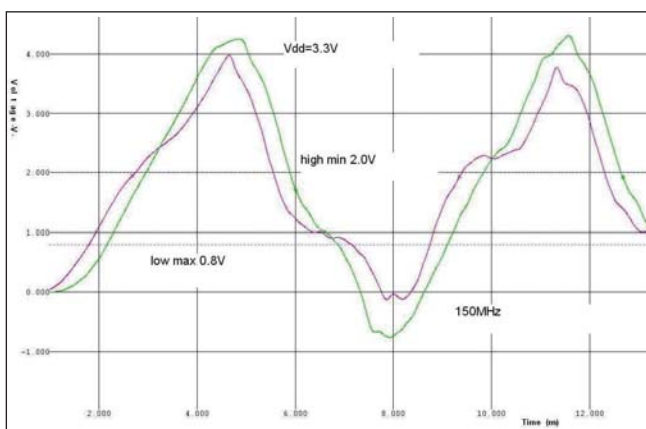


Figure 3. The circuit works at 150MHz but does not work at 200MHz.

B. Simulation Approach

LineSim of Hyperlynx has a facility called Terminator Wizard that can provide suggestions on termination resistance values for a number of termination techniques such as series, parallel, and Thevenin terminations [11].

An example circuit from [8] is used to show the effectiveness of the Terminator Wizard as shown in Figure 4. The voltage at the receiver input C0 in Figure 4 are displayed in the eye diagram in Figure 5 to show how much distortion each termination technique might introduce after applying resistance values for corresponding terminations recommended by the Terminator Wizard.

The eye diagrams in Figure 5 are configured so that the top line is at 3.3V and the bottom line at 0V. The diamond has the slope of 0% to 10% and 90% to 100%, and the high and low threshold voltages of 2V and 0.8V.

As can be seen from Figure 5, overshoots at both high to low and low to high transitions were more than 1V when there is no termination resistor. This was because of the reflections due to high input impedance of the load. Series termination reduced the overshoot to bare minimum but caused longer rise time delay since the time constant was increased by the series termination resistor.

Parallel termination introduced less rise time delay but the pullup resistor of 39.1 ohm caused logic low state to be lifted to be close to 0.8V, which was the upper bound of the logic low state. The circuit had therefore almost 0V noise margin at low state and could be sensitive to noises. Thevenin termination produced similar waveforms as these of parallel termination with better noise margins at both high logic state and low logic state.

IV. UNDERSTANDING FACTORS OF CROSSTALK

Crosstalk refers to induced voltage or current in a circuit due to electric field or magnetic field coupling from adjacent circuits. Coupling estimation between two circuits is needed in order to understand crosstalk.

Traditional theoretical formula-based approach to crosstalk analysis can only deal with linear models and regular structures and is inadequate to treat the distributed effects in real circuits while PCB simulation with IBIS models can deal with more complex and realistic circuits [13]–[15].

A. Traditional Approach

In theory, electric field or capacitive coupling can be modeled as a dependent current source and magnetic field or inductive

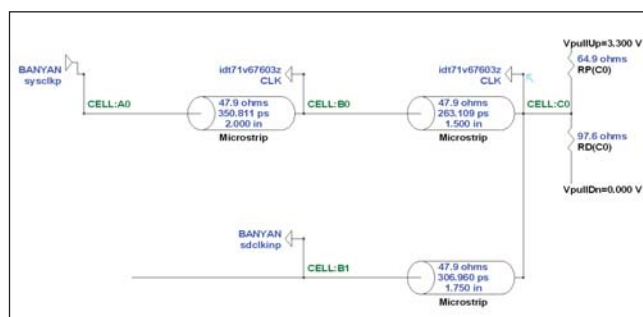


Figure 4. The Thevenin termination circuit.

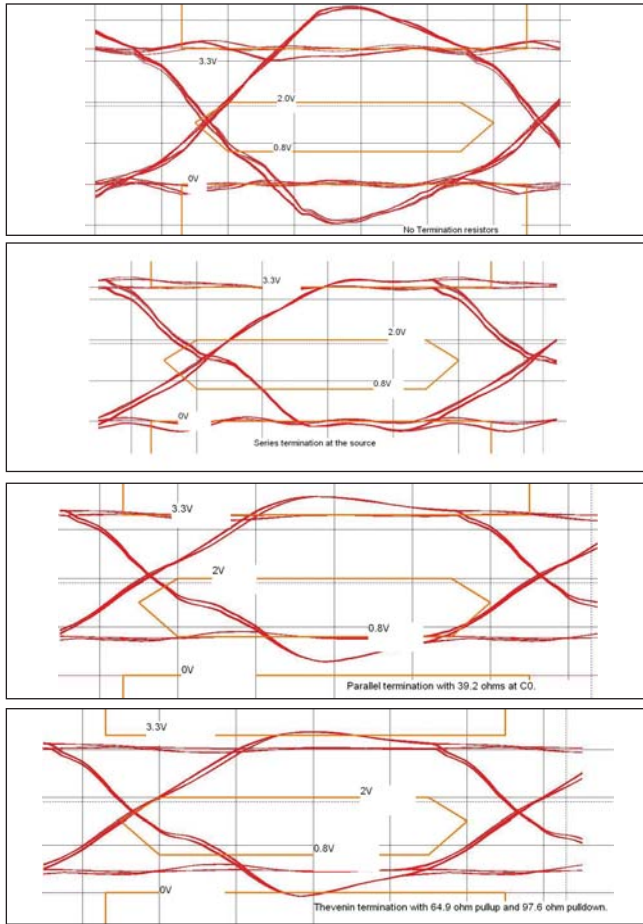


Figure 5. Signals at clock driver and receiver with various terminations.

coupling a dependent voltage source. The details of this approach can be found in [12].

Near-end crosstalk due to capacitive coupling can be estimated by $V_{NE,CAP} = \frac{1}{4} \frac{C_m}{C} V_o$, where C is per-unit-length capacitance of the trace, C_m is per-unit-length mutual capacitance, and V_o is the amplitude of the source voltage. Far-end crosstalk due to capacitive coupling can be estimated by $V_{FE,CAP} = \frac{1}{2} Z_0 C_m d \frac{V_o}{t_r}$, where C_m is per-unit-length mutual capacitance, and V_o is the amplitude of the source voltage, Z_0 is the characteristic impedance, d is time-of-flight, and t_r is the rise time of the source voltage.

Near-end crosstalk due to inductive coupling can be estimated by $V_{NE,IND} = \frac{1}{4} \frac{M}{L} V_o$, where L is per-unit-length inductance of the trace, M is per-unit-length mutual inductance, and V_o is the amplitude of the source voltage. Far-end crosstalk due to inductive coupling can be estimated by $V_{FE,IND} = \frac{1}{2} MD \frac{V_o}{2t_r}$, where M is per-unit-length mutual inductance, and V_o is the amplitude of the source voltage, Z_0 is the characteristic impedance, d is time-of-flight, and t_r is the rise time of the source voltage.

B. Simulation Approach

Crosstalk between traces on a PCB can be estimated with LineSim and the results can be compared with theoretical analysis. This exercise helps students to understand the limit and conditions under which the theory of crosstalk analysis

holds as well as to have the freedom of exploring design space parameters to see how crosstalk changes.

In the following example, a simple two-trace crosstalk coupling is evaluated both theoretically and with LineSim simulation. The circuit and its simulation results are shown in Figure 6.

From LimSim, we can find $C = 86.6$ pF/m, $C_m = 24.9$ pF/m, $L = 396.5$ mH/m, $M = 163.3$ mH/m, $V_o = 3V$, and $t_r = 1$ ns. Therefore, the estimated crosstalk components are

$$V_{NE,CAP} = 215.6mV; \quad V_{FE,CAP} = 670mV;$$

$$V_{NE,IND} = 308.7mV; \quad V_{FE,IND} = -882.5mV.$$

The total near-end and far-end crosstalk is simply the sum of the two contributors. Therefore $V_{NE} = 524.2mV$ and $V_{FE} = -212.5mV$.

Figure 6 gives simulation results that show that the theoretical prediction for near-end crosstalk agrees with the simulation result well but that for far-end crosstalk does not match the simulation result.

V. CONCLUSION

A number of examples of signal integrity evaluation with simulation by LineSim of Hyperlynx are presented in which the results from closed-form analysis are then compared with simulation. Our experience has shown that LineSim is an effective tool that helps students understand conceptual issues in signal integrity and which helps them in exploring design options for maintaining signal integrity. The simulation approach therefore complements and augments traditional theoretical analysis.

Because of its simplicity, intuitive approach, and affordability, LineSim of Hyperlynx is a valuable tool in teaching signal

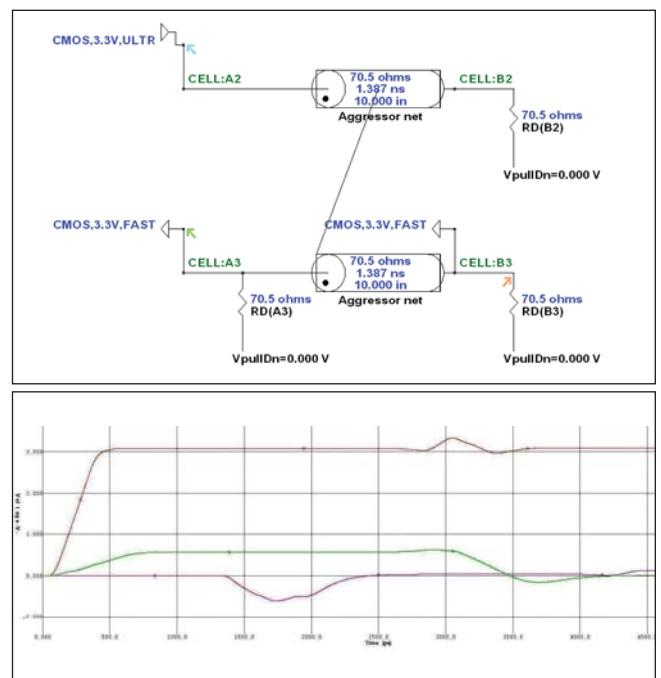


Figure 6. Simple near- and far-end crosstalk between two traces.

integrity for high-speed digital system implementation on a printed circuit board. The tool has been used to evaluate design guidelines from various companies [16]–[18] and to explore optimal design space with large and practical designs such as USB devices and RAMBUS.

Simulation tools for signal integrity at PCB level have become affordable, accurate and straightforward to use. They are valuable tools to expand student experience in high-speed design classes. They have also become a necessity in introducing new approaches to signal integrity problems in the classroom.

Equally importantly, these tools can be used to introduce a greater percentage of computer engineers and digital designers to the importance of PCB layout and design in the performance of high-speed circuits, critical audiences to enable the efficient design and manufacture of high-speed circuits.

Looking to the future, introducing these topics into more areas within electrical and computer engineering curricula promises a workforce having greater awareness of the needs and challenges inherent in high-speed design.

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Biographies



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