



Volume 7
Number 1
January 2002

SOLID-STATE CIRCUITS

IEEE Solid-State Circuits Society Quarterly Newsletter



ICs for Information Technologies, ISSCC 2002

Our lives have been, and continue to be, affected dramatically by the multitude of portable and table-top devices created for improved communications. We constantly are informed about news events, the stock market, and whoever or whatever we want to focus on. Information has become a commodity for many of us. This is a result of the new ICs that have been conceived and developed by the IC community to provide ever-growing

capabilities at increasing speed and performance. As in other years, ISSCC 2002 provides the best available overview of the new ICs that have emerged this year, and that are destined to influence current and future markets.

The International Solid-State Circuit Conference will be held 3-7 February 2002 at the San Francisco Marriott Hotel. Tutorials, a workshop, and special evening sessions are available on Sunday, 3 February 2002.



ISSCC REGISTRATION ALERT

Our original registration agency has gone out of business. Conference registration instructions appearing in the mailed ISSCC Advance Program are no longer valid. Go to www.isscc.org for corrected registration instructions. Hotel registration remains unchanged.

this IN issue

- Retrospective of ESSCIRC 2001* 5
- August SSCS AdCom Meeting* 6
- John W.M. Rogers Receives 2001-2002 SSCS Predoctoral Fellowship* 7
- New Senior Members* 7
- Five New 2002 AdCom Members* 8
- Call for Nominees for SSCS AdCom* 9
- Retrospective on the 2001 Symposium on VLSI Circuits* 10
- Chapters Update* 11
- Invest in Yourself: Remember to Renew* 13
- Invest in a Colleague: Nominate an IEEE Fellow* 13
- Invest in the Profession: Make a Nomination for the SSCS Award* 14
- Find Out What's Happening* 15
- Journal Table of Contents Via Email* 15
- SSCS Events Calendar* 16

Plenary Speakers

Three invited papers will begin the Plenary Session Monday morning. Dennis Buss, Vice-President, Silicon Development, Texas Instruments, Dallas, Texas, will talk about "Technology in the internet era." In his view, internet electronic products, not PCs alone, drive IC technologies. Internet products need less computational power than PCs but better portability and cheaper cost to penetrate mass markets. SOCs will integrate everything including radio and wireline drivers, and Moore's law will continue for another decade.

C.G. Hwang, CEO, Samsung Semiconductor Memory Division, Yongin-City, Korea, will speak on "Semiconductor memories for IT." He feels servers will continue to drive high-density DRAMs with 16-Gb DRAMs

expected this decade. Now memory is driven by graphics and networking applications. Low-power memory is driven by 3G phones and PDAs. He also believes Moore's law will continue for another decade.

Fred Boekhorst, Senior Vice-President, Philips Research, Eindhoven, Netherlands, will talk on "Ambient intelligence: The next paradigm for consumer electronics." Ambient intelligence refers to an environment where the user experience is what matters. People want to have fun, to be in control, and to be productive. This is not linked to one particular device but a network of on-body devices that allow new experiences. The three driving directions are radio, user interface, and visual display.

Continued on next page

Five new 2002 AdCom members (page 8)

Contributed Paper Sessions

The Program Committee evaluated over 350 papers submitted from around the world and selected 171, with authorship equally divided among the United States, Europe, and the Far East. Over three-quarters of the presentations are industry papers with one-quarter from Universities. The papers are grouped into eight major topics and presented over three days in 25 sessions with five simultaneous sessions. Registrants may look for these and other highlights as they examine their Advance Program, available on-line at www.isscc.org.

Analog

Session 10 on Tuesday morning will unveil an 8-bit ADC operating at 4 Gigasamples per second, a 20-fold increase in sample rate. Surprisingly, this result has been achieved in 0.35 μ m CMOS. Formerly, such performance was available only in the realm of expensive processes such as SiGe and GaAs. This ADC will provide a critical jump in the performance of lead-edge test equipment.

In Session 18 on Wednesday morning the lowest-ever voltage supply to power an Sigma-Delta ADC will be reported at 0.7 V. Normally ADCs switch the filter capaci-

| ISSCC 2002 Schedule of Session Topics | Monday afternoon | Tuesday morning | Tuesday afternoon | Wednesday morning | Wednesday afternoon |
|---------------------------------------------|---------------------|--------------------|----------------------|----------------------|------------------------|
| Analog | | 10 | 13 | 18 | 23 |
| Digital | | 8 | 16 | 20 | 25 |
| Imagers, Displays and Mems | 2 | | | | 26 |
| Memory | 6 | 9 | | | |
| Signal Processing | 3 | 7 | | | 22 |
| Technology Directions | | 11 | 12 | 21 | |
| Wireless Communications | 5 | | 14 | 17 | 24 |
| Wireline Communications | 4 | | 15 | 19 | |

tors and require 1.5 V. This ADC design switches the entire operational amplifier, which allows the lower supply voltage. Conventional CMOS processing can be used and the filter capacitors are provided by the inherent capacitances of the transistors themselves.

Session 23 on Wednesday afternoon introduces, for the first time, a disposable chip for hearing aids. It utilizes many low-power, low-voltage analog-circuit techniques and provides 40 days of average use with a small zinc-air battery.

Digital

With four sessions on digital topics, there will be coverage throughout Tuesday and Wednesday. Attendees will hear about the introduction of 0.13 μ m technology in product roll-outs of the next-generation Power PC in Session 8 on Tuesday morning and Ultrasparc in Session 20 Wednesday morning. Technology trends in extending microprocessor performance are also evident in the move to body-bias solutions which reduced standby power in one CMOS communications router by a factor of 3.5. Body-bias is proposed in numerous papers, in particular during Session 16 on Tuesday afternoon and Session 25 on Wednesday afternoon.

With the scaling of silicon-process technology confronting fundamental limitations, more pressure is being focused on the means of achieving performance beyond simply increasing frequency. Primarily this is achieved by getting the microprocessor to do more per clock cycle. For example, in Session 8 on Tuesday morning there are two reports on clock-distribution systems for centimeter-square-sized die with skew reduced below 25 ps. In addition, several papers highlight the latest chip system organizations, including huge and complex on-chip caches,

ISSCC Special Topic Sessions:

Next-Generation Circuit-Design Challenges

Sunday evening (new this year)

- Inductance: Implications and Solutions for High-speed Digital Circuits
- Low-Voltage Design for Portable Systems

Evening Panel Discussions

Monday

- Software Radio: Cool or to be Cooled?
- When Will Optical Interconnects Impact Microprocessors?
- Does Moore's Law Apply to Analog?
- Have Universities Killed Research or Has Industry Corrupted It?

Tuesday

- Low-Voltage Design or the End of MOSFET Scaling?
- SOI: Solution or Indigestion?
- * What Caused the Telecom Crash?
- * Solid-State Circuits: System or Circuit Innovation?

expanding banks of execution units, and multithreading. For example, Session 20 on Wednesday morning will report the latest superscaler multithreaded Alpha processor with 2.5 to 3 times the performance of previous generations using over 3 MB of on-chip cache.

Embedded designs for System-on-a-Chip building blocks that will be presented during Session 20 on Wednesday morning are characterized by a device count of approximately 5 million transistors, die sizes of under 75 mm², and power consumption of no more than 0.5 watts. Performance will be shown to reach 400 MHz. This kind of performance represented the best-of-breed processor performance less than 5 years ago!

Imagers, Displays, and MEMS

Session 2 on Monday afternoon will focus on adding functionality to both CMOS and CCD devices, rather than the usual pursuit of larger chip size, higher resolution, or greater image quality. With sensors there is little sense of the “traditional” CMOS vs CCD arguments as CMOS and CCD sensors have each found their own niche application areas. CCD sensors continue to add functions in order to remain competitive in a world of low-cost CMOS devices threatening their dominance of the digital still-camera market.

Session 26 on Wednesday afternoon will focus on the interface between the ‘real’ world and the ‘digital’ world. The signals vary from mechanical (in accelerometers and gyroscopes), to chemical (in volatile-organic compound sensors), to thermal (in wind monitors), to light (in imagers and displays). Micromachin-

Workshops, Tutorials and Short Courses

Sunday SSCTC Workshop

Analog Telecom-Access Circuits and Concepts

Sunday Tutorials

Attendees may register for a maximum of three tutorials. Taught by experts from the Program Committee, these 90-minute sessions meet attendees’ needs for introductory material in the respective topics. These sessions fill up fast.

Image Sensors

Reliability

Mixed Signal

FeRAM

Cryptography

Wireless

Gb/s Data

Thursday Short Course

Wideband Communications

Thursday Workshop

Microprocessor Design Workshop

ing technologies are used to realize sensor elements that could not be implemented using conventional IC technology. This session will report the first fully functioning solid-state micromechanical gyroscope. This compact industrial-quality system incorporates a large number of on-chip signal-processing circuits along with mechanical parts. The world’s first organic light-emitting microdisplay (OLED) on silicon will also be reported. This low-power color display will enable such systems as head-mounted displays and other near-to-eye implementation such as ‘Dick Tracy’ watches.

Memory

Session 6 on Monday afternoon will report the first 1-Gb 1-bit-per-cell NAND Flash memory. High-density general-purpose memories expand across broad applications providing lower-cost, higher-density non-volatile mass storage.

Session 9 on Tuesday morning will show the highest-density ferroelectric memory reported to date. The 8 Mbit barrier in ferroelectric memory has been broken by a 3.0-V 32 Mb FeRAM, implemented for static data storage in a 0.25µm

process. The reported density gives FeRAM a competitive edge compared with SRAM, which has peaked at 16 Mbit density. The memory implements an SRAM-like asynchronous interface by using address-transition detection to generate internal clock signals. SOI technology is also shown to offer smaller, more efficient DRAM cells with non-destructive read capability.

Signal Processing

The deployment of advanced wireless systems and continuing advances in storage density and bandwidth necessitate similar advances in digital signal processors and circuits. In Session 3 on Monday afternoon the first 10-Gb switching processor for high-speed internet will be introduced. Also, two out of three high-performance DSPs for 3G wireless base-stations will be described in this session; look for a third 3G device during Session 7 on Tuesday morning. A two-chip IEEE802.11a solution will also be presented.

A variety of multimedia devices will be presented in Session 22 on Thursday afternoon, covering 3G and MPEG4. The three lowest-power video codecs in active and standby mode will be presented for portable applications. They use a high level of circuit integration and relatively low clock speeds to reduce power consumption.

Technology Directions

In Session 12, Digital Directions, several emerging technologies that could reduce costs and lower the power consumption of future digital designs will be presented. A super-computer System-on-a-Chip project will be described. Using energy-efficient and area-efficient embedded-

processor cores, it becomes possible to place two processors plus the upper three levels of the memory hierarchy on a single chip. This chip can be arrayed to build a supercomputer containing hundreds of thousands of processors with cost and power consumption much lower than a design based on conventional desktop and server microprocessors.

Ovonic technology, previously used mostly for solar-energy conversion, will be combined for the first time with conventional CMOS to yield a dense, fast, low-voltage non-volatile 4 Mbit memory. It stores information as a phase change between amorphous and polycrystalline states, similar to the technique in rewritable CD and DVD technology. Also in this session, on-chip global diagonal routing is demonstrated on a 128-bit RISC processor that shows a 19.8% path-delay reduction and a 10% area reduction.

For the past few years ISSCC has been the primary venue for presenting the latest developments in highly integrated ICs for fingerprint sensing and analysis. Session 21 on Wednesday morning will report two papers describing single-chip integrated solutions for low-cost high-volume markets, such as consumer fraud prevention and security. Remote sensing of vital signs with a fully integrated direct-conversion Doppler radar for noninvasive detection of heart rate and respiration will be reported in combination with its 1.6-GHz transceiver. Very exciting developments in the field of bioMEMS and DNA analysis chips also will be reported in this session: a 16X8 DNA sensor array with a fully-electronic readout scheme on top of a standard DMOS chip without the need for optical components will allow low-cost and high-performance fabrication.

Wireless Communications

Session 5 on Monday afternoon will feature several outstanding presentations in the areas of Bluetooth

integration and cost reduction as well as IEEE 802.11a, the newest of the deployed wireless-LAN technologies. The first fully integrated 802.11a radio will also be presented in this session.

Presentations on cellular telephone RF functions on a single IC (excluding power amplifiers) are scheduled for Session 14 on Tuesday afternoon. Several state-of-the-art advances in integration, improvements in performance levels, and additional functionality will be reported. An example is a cellular RF chipset with an added GPS receiver.

Advanced RF techniques, on Wednesday morning in Session 17, presents a number of solutions to the integration challenge of the VCO due to phase-noise issues. Also at this time look for startling advances in integration of systems operating in excess of 50 GHz. There is an IC wireless transceiver handling data at optical-fiber rate speeds (1.25 Gb/s) in a wireless environment. Operating at a data rate of 1.25 Gb/s at a frequency of 60 GHz, it uses a band which is 25 times higher in frequency than Bluetooth or other popular LANs. A fully integrated VCO at 51 GHz using low power will also be presented. Using standard 0.12 μ m CMOS technology, this device will support wireless portable handsets in band enabling these wide 1 Gb/s data rates.

All the papers in Session 24 on Wednesday afternoon will demonstrate the growing acceptance of CMOS as an RF technology because of its ability to provide acceptable RF performance at low cost, as well as its amenability to integrate with digital blocks. A highly integrated broadband cable-tuner IOC in 0.35 μ m CMOS and a single-chip CMOS GBS receiver with the lowest power consumption to date will be presented.

Wireline Communications

To satisfy the increasing demand for backplane interconnect bandwidth, papers on serializer/deserial-

izer (SerDes) technology in Session 4 on Monday afternoon will show significant improvements on several fronts, namely power consumption down to 86-mW per SerDes channel, unprecedented integration, and reduced jitter.

Tuesday afternoon's Session 15 will present papers showing how optical communication systems continue to move towards 10- to 40-Gb/s rates. Prior 10-Gb/s SONET required GaAs or SiGe ICs, which increased system cost and complexity. Low-cost 10- to 40-Gb/s Ethernet datacom systems now match the data rate of OC 192 SONET telecom systems. SONET survival requires aggressive cost reduction in SONET system designs. The novel contributions stepping up to that challenge are the first fully-integrated OC-192 transmitter and receiver realized in standard 0.18 μ m CMOS. The highest bit-rate ever reported for 4:1 MUX and 1:4 DEMUX circuits in 0.2 micron SiGe BiCMOS will enable >50 Gb/s optical systems. New techniques for implementation of 10-Gb/s CDRs for SONET OC-192 and DM applications will improve jitter and enable use of lower-cost technologies.

VDSL technology is expanding the DSL bit rate by an order of magnitude for short-loop applications. Wednesday morning's Session 19 will feature two different approaches on architectures and circuits for low-power central-office line drivers for Discrete-Multi-Tone (DMT) ADSL, taking advantage of a high-performance trench isolated complementary-bipolar process. This session will also describe the first two published implementations of the analog-front-end ICs for the recently adopted DMT-based 4-band VDSL standard. This standard specifies up to 12 MHz of analog bandwidth and partitions the spectrum into two downstream bands and two upstream bands. Note that both implementations require external line drivers and other external line-interface circuitry. ●

Retrospective of ESSCIRC 2001

The European Solid-State Circuits Conference (ESSCIRC 2001) was held 18-20 September in Villach, Austria, a hotbed for microelectronic activities. The conference was a success, with 362 registered participants from 22 countries. Unfortunately, 30 registrants cancelled in the aftermath of the terrorist attacks of 11 September 2001. The conference was a first-class international forum for circuit designers to discuss practical aspects of integrated-circuit design. The technical program included 8 invited papers, 98 regular papers, and 31 posters, which were selected out of 196 submitted contributions from all over the world.

Invited Presentations

The keynote address, given by Willy Sansen of KUL, was titled "SOC design from a mixed-signal perspective." He described the various performance-limiting effects and emphasized that achievable analog performance still relies both on the art of making the correct compromise and the experience that has been built up over decades.

Wolfgang Pribyl of Austria Mikro Systeme explored the position of silicon foundries for mixed-signal services and sketched the major success factors and future chances for small- and medium-sized foundries.

Andreas Kaiser of IEMN-ISEN presented the "Potential of MEMS components for reconfigurable RF interfaces in mobile communication terminals."

Yoshiaki Hagiwara of Sony, Tokyo gave a fascinating description of what we can expect for future homes in "Microelectronics for home entertainment." Due to events of 11 September, he could not attend in person, but his presentation via a conference connection was exemplary and well received.

Stefan Rusu of Intel presented "Trends and challenges in VLSI technology scaling towards 100

nm," in which he outlined the challenges and achievements that lie ahead for integrated circuits in the next decade. He concluded that there is no fundamental barrier to prevent the extension of Moore's law into the next decade.

Josef Hausner of Infineon, Munich, talked about "Integrated circuits for next-generation wireless systems," explaining the challenges and requirements of integrated circuits as the enablers for the new Universal Mobile Telephone System (UMTS).

Chris Rowen of Tensilica showed the capabilities of "Automated Processor Generation for System-On-A-Chip" design. He concluded that new methodologies, tools, and processor foundations will be required for the shift to application-specific processors with the efficiency of application-tuned silicon.

Finally, Leonard Gagea of TTChip, Vienna, explained and analyzed the architecture of communication buses for safety-critical applications like x-by-wire systems.

Technical Program

The outstanding technical program included topics on Synthesizers, Modulators/Demodulators, Systems On A Chip, Digital Systems, Optical Circuits, Memory and Interface Circuits and Circuit Design Techniques. Keeping with tradition, the contributions were dominated by mixed-signal and RF papers like Voltage Regulators, RF/IF Amplifiers, Data Converters, CMOS Imagers, and Power Circuits.

In the RF area one of the highlights was "A CMOS 10-GHz voltage-controlled LC-oscillator with integrated high-Q inductor," by W. De Cock and M. Steyaert of KUL, analyzing the sources of Q-degradation. In this realization the Q of the integrated inductor is not the limiting factor any more and the reported phase noise performance of -127 dB/Hz at a frequency offset of 3 MHz in CMOS is an excellent result. Equally interesting was the

"Injection locking scheme for precision quadrature generation," presented by R. Melville of Agere. Here, the principle of injection locking, described some 60 years ago, is used to yield excellent performance of ring oscillators, which otherwise exhibit high phase noise.

In the data converter arena, much attention was given to band-pass Delta-Sigma ADCs, with two interesting contributions from T. Salo et al. of Helsinki University of Technology about "An 80-MHz band-pass delta-sigma modulator for a 100-MHz IF-receiver" and "A fourth-order band-pass delta-sigma modulator using second-order band-pass noise-shaping dynamic element matching" by T. Ueno et al. from Toshiba. Highly integrated mixed-signal circuits were reported in several papers, such as the fully "Integrated analog front-end macro for cable modem applications in 0.18- μ m CMOS" from A. Wiesbauer et al. of Infineon.

In optical communications a tendency for even higher speed and a high level of integration using deep sub-micron CMOS was observed. Good examples in this area were the papers from A. Younis et al. from RocketChips/Xilinx about a "Low jitter, low power, CMOS 1.25-3.125 Gb/s transceiver" and the "Fully integrated CMOS light to logic fiber-optic receiver circuit" from K. Schrödinger et al. of Infineon. The paper "High-speed CMOS analog Viterbi detector for 4-PAM partial response signaling" by B. Zand et al. of the University of Toronto describes a high-speed mixed analog-digital partial response Viterbi decoder. Of interest is the combined analog branch-metric and add-compare-select unit.

On the subject of memories, H. Kikukawa et al. of Matsushita and Mitsubishi presented "A 0.13 μ m 32 Mb/64-Mb embedded DRAM core with high efficient redundancy and enhanced testability" in a 0.13- μ m triple-well 4-level copper embedded

Retrospective of ESSCIRC 2001 *continued*

DRAM technology. "A 1Kx1K high dynamic range CMOS image sensor with on-chip programmable region-of-interest readout" by O. Schrey et al. of the Fraunhofer Institute in Duisburg highlighted the important domain of sensors for machine vision applications. Finally A. Lelah et al. from France Telecom & ENST presented "A CMOS VLSI pilot and support chip for a liquid crystal on silicon 8x8 optical cross-connect demonstrator," suitable for high-speed WDM transport networks.

Banquet Address

One of the most entertaining and well-received presentations was given by Shyam Kamath of California State University, Hayward, titled "What is Silicon Valley's success based on: silicon or entrepreneur-

ship?" It placed silicon and entrepreneurial attitude face-to-face, combining economics with managerial aspects.

Educational Sessions

Two educational sessions were given, one before and one after the conference. The workshop "System On Chip" emphasized networks on chip, intrinsic computing efficiency, grain size, reconfigurable hardware and RF systems on chip. It was presented by A. Jantsch, J.P. Soinen, M. Forsell, and S. Kumar of KTH, Sweden; M. Millberg and J. Ölberg of VTT Electronics, Oulu, Finland; J. Huisken of Philips, The Netherlands; and M. Steyaert of KUL, Belgium. The tutorial "Electronics for automotive" covered smart power semiconductors for innovative automotive solutions,

future automotive communication architectures, and innovative SOI technology for 12-V/42-V power supplies. It was presented by H. Zitta and C. Preuschoff of Infineon and C. Mochel of Atmel, Germany.

Details about purchasing the Proceedings of past ESSCIRC conferences are available at www.esscirc.org/proceedings.htm

ESSCIRC 2002 and ESSDERC 2002 will be held jointly 24-26 September 2002 in Florence, Italy (ele.unipv.it/esscirc2002) ●



Franz Dielacher
Technical Program
Chair
ESSCIRC 2001
Franz.dielacher@infineon.com

August SSCS AdCom Meeting

The second 2001 SSCS Administrative Committee meeting was held 27 August in San Francisco, California, to review the Society's operations and take action on new activities. The following actions were taken:

Microwave Conference and Publication

The Society will provide technical co-sponsorship of the Radio Frequency Integrated Circuits Symposium in 2002. The RFIC will meet 2-4 June 2002 in Seattle, Washington, in conjunction with the International Microwave Symposia. Other sponsors of RFIC include the IEEE Microwave Theory and Techniques Society and the IEEE Electron Devices Society.

The AdCom decided against financial support for a special issue of the IEEE Transactions on Microwave Theory and Techniques.

Originally scheduled to come out in fall of 2001 with a focus on integrated and nonintegrated silicon RF and microwave circuits, the special issue has now been expanded to include a 50-year history of MTT. This increased scope has delayed publication until winter of 2002. Since most SSCS members interested in this issue are probably already members of MTT, the cost of printing and distributing the issue to the full SSCS membership was judged unnecessary. Members who are interested in this issue are welcome to subscribe to the IEEE Transactions on Microwave Theory and Techniques.

Finances

In an email ballot prior to the August meeting, the AdCom agreed to increase the 2002 nonmember subscription price of the JSSC to \$445. The rate has remained at \$380

for three years, increased from \$300 in 1998, and still remains well below prices of similar technical publications. Most libraries purchase a package of all Society periodicals (ASPP) and do not purchase individual subscriptions at this individual nonmember price. ASPP customers enjoy an additional discount of roughly 40% from nonmember prices.

The AdCom felt it necessary to increase the SSCS dues for 2003 to \$20. The increase was in response to the current IEEE financial environment. SSCS has been the least expensive IEEE Society with a technical publication bundled into the dues and, at the increased membership rate, will remain among the least expensive. Other financial actions included loaning \$35,000 in seed money for the 2002 Symposium on VLSI Circuits and providing \$18,400 in subsidies for projects undertaken by 23 SSCS Chapters. ●

Solid-State Circuits is online

Find us at www.sscs.org

John W. M. Rogers of Carleton University Receives 2001-2002 SSCS Predoctoral Fellowship

John W. M. Rogers, a doctoral candidate at Carleton University, Ottawa, Canada, has been selected to receive the second IEEE Solid-State Circuits Society Predoctoral Fellowship for 2001-2002.



Born in Cobourg, Ontario, Canada, in 1974, Rogers received his BE degree in 1997 and his ME degree in 1999, both in electrical engineering, from Carleton University. During his ME degree research

he was a resident researcher at Nortel Networks' Advanced Technology Access and Applications Group, where he performed exploratory work on VCOs for personal communications. During that same period he was involved in the development of a Cu interconnect technology for building high-quality passives for RF applications. He is currently collaborating with SiGe Semiconductor Ltd. in Ottawa while pursuing his PhD at Carleton

University under the supervision of Professor Calvin Plett. His research interests are in the areas of RFIC design for wireless and broadband applications. Mr. Rogers received the BCTM best student paper award in 1999, has four U.S. patents pending, and is a member of the Professional Engineers of Ontario.

An award certificate will be presented to Mr. Rogers at the International Solid-State Circuits Conference (ISSCC) during the opening morning Plenary Session at the San Francisco Marriott on Monday, 4 February 2002. ●

Congratulations to New Senior Members

Babak Bastani
 Edgar H. Callaway
 Anantha Chandrakasan
 Yaochung Chen
 Won-Jae Choi
 Joseph A. Devore
 Milos D. Ercegovic
 Gary K. Fedder
 Adel Ghazel
 Yin Hu
 Dimitris E. Ioannou
 Koichiro Ishibashi
 Daniel B. Jackson
 Takamaro Kikkawa
 Jente B. Kuang
 Di-Son Kuo
 Jong Ho Lee
 Junichi Nakamura
 Dimitris C. Pantelakis
 V. J. Rao Rapeta
 J.N. Roy
 Stefan Rusu
 Takayasu Sakurai
 John L. Schmalzel
 Tsugumichi Shibata
 Jai-Hoon Sim
 Ganapathy Subramaniam
 Hiroshi Takahashi
 John R. Tower
 John T. Trnka
 Surya Veeraraghavan
 Jeff Watt
 Danny R. Webster
 Kyoungsoon Yang
 Choh-Fei Yeap
 Hyun-Kyu Yu

IEEE Solid-State Circuits Society AdCom

President:

Charles G. Sodini
 Massachusetts Institute of Technology
 Cambridge, MA
 sodini@ntl.mit.edu
 Fax: +1 617 253 8806

Vice President:

Stephen H. Lewis
 University of California
 Davis, CA

Secretary:

Asad Abidi
 University of California
 Los Angeles, CA

Treasurer:

David Hodges
 University of California
 Berkeley, CA

Past President:

Bruce Wooley
 Stanford University
 Stanford, CA

Elected AdCom Members at Large

Terms to 31 Dec. 02:
 Anantha Chandrakasan
 John Corcoran
 Chris Mangelsdorf
 Willy Sansen
 Christer Svensson

Terms to 31 Dec. 03:

Asad Abidi
 Bryan Ackland
 Gary Baldwin
 David Hodges
 Kiyoo Itoh

For questions regarding Society business, contact the SSCS Executive Office.

Contributions for the April 2002 issue of the newsletter **must be received by 28 January 2002** at the SSCS Executive Office.

Anne O'Neill, Executive Director
 IEEE SSCS
 445 Hoes Lane, P.O. Box 1331
 Piscataway, NJ 08855-1331

Tel: +1 732 981 3400
 Fax: +1 732 981 3401
 Email: sscs@ieee.org

Terms to 31 Dec. 04:

Gerhard Fettweis
 Richard C. Jaeger
 David A. Johns
 Takayasu Sakurai
 Neil Weste

Other Representatives:

Representative from CAS to SSCS
 Edgar Sanchez-Sinencio
 Representative to CAS from SSCS
 Neil Weste

Chairs of Standing Committees:

| | |
|--------------|---------------------|
| Awards | Richard C. Jaeger |
| Chapters | Jan Van der Speigel |
| Meetings | Mark Horowitz |
| Membership | Jonathan David |
| Nominations | NA |
| Publications | Richard C. Jaeger |

Solid-State Circuits Technology

Committee Cochairs:

Stan Schuster
 Steve Garverick

Newsletter Editor:

Lewis M. Terman
 IBM Somers
terman@us.ibm.com
 Fax: +1 914 766 2814

For detailed contact information, see the Society Web page: www.sscs.org/info/

Five New 2002 AdCom Members

The SSCS membership elected five AdCom members in the Fall 2001 election. As has been the case in all elections for the AdCom of the Solid-State Circuits Society, the vote totals in this year's election were quite close. Every candidate on this year's outstanding slate received a significant number of votes from our membership.

The following candidates have been elected:

Gerhard Fettweis
Richard C. Jaeger
David A. Johns
Takayasu Sakurai
Neil Weste

For the electees, the term of office starts on 1 January 2002 and lasts for three years.

I thank all the candidates who agreed to run for this office. They are all outstanding contributors to the SSCS, and I look forward to having each engaged in the Society's activities in the future. The success of the Society depends on the efforts and dedication of individuals such as these and their willingness to commit their time and expertise to the benefit of all of the members of our profession. We are deeply in their debt.



Bruce Wooley
SSCS President
Wooley@par.stanford.edu

Gerhard Fettweis received his MSc/Dipl-Ing and PhD degrees in EE from the Aachen University of Technology (RWTH), Germany, in 1986 and 1990, respectively.

From 1990 to 1991 he was a Visiting Scientist at the IBM Almaden Research Center in San Jose, California, working on signal processing for disk drives. From 1991 to 1994 he was a Scientist with TCSI, Berkeley, California, responsible for signal-processor developments for mobile phones. Since September 1994 he has held the Mannesmann Mobilfunk Chair for Mobile Communications Systems at the Dresden University of Technology, Germany. He has been an elected member on the SSCS Administrative Committee since 1999, and on the IEEE ComSoc Board of Governors from 1998 to 2000. He has been Associate Editor for *IEEE Transactions on Circuits and Systems II*, and Associate Editor for *IEEE Journal on Selected Areas in Communications*, the wireless series. Over the years he has organized and been on the program committees of numerous IEEE workshops and conferences. Since 1999 he has been CTO of Systemonic, a startup spun out of TU Dresden, focussing on broadband wireless chipsets.



Richard C. Jaeger received his BS and ME degrees in EE in 1966 and his PhD degree in 1969, all from the University of Florida, Gainesville. From 1969 to 1979 he was with the IBM Corporation working on precision analog design, PL, microprocessor architecture, and low-temperature MOS device and circuit behavior. Since 1979 he has been at Auburn University where he is Distinguished University Professor in Electrical and Computer Engineering. In 1984 he helped found the Alabama Microelectronics Science and Technology Center and served as Director of the center until 2000. He has published over 200 technical papers and articles and three books: *Introduction to Microelectronic Fabrication*, *Microelectronic Circuit Design*, and *Computerized Circuit Analysis Using SPICE Programs* with B. M. Wilamowski. From 1980 to 1982 he served as founding Editor-in-Chief of *IEEE MICRO*. He was elected Fellow of the IEEE in 1986.

Dr. Jaeger was a member of the IEEE Solid-State Circuits Council from 1984-1991, serving the last two years as Council President. He was Program Chair for the 1993 International Solid-State Circuits Conference, Chair of the 1990 VLSI Circuits



Symposium, and Editor of the *IEEE Journal of Solid-State Circuits* from 1995-1998. He has been an elected member of the SSCS AdCom since 1999, and Chairs the SSCS Publications and Awards Committees.

David A. Johns received the BAsC, MASc, and PhD degrees from the University of Toronto, Canada, in 1980, 1983 and 1989, respectively.

In 1988 joined the University of Toronto where he is currently a full Professor. He has ongoing research programs in analog integrated circuits with particular emphasis on digital communications, oversampling, signal processing, PLLs, ADCs, DACs, and adaptive filtering. His research work has resulted in more than 40 publications as well as the 1999 IEEE Darlington Award. He is co-author of the *Analog Integrated Circuit Design* (Wiley, 1997) textbook and has given numerous industrial Short Courses. In addition to his academic experience, he has four years of semiconductor industrial experience during 1980, 1983-85, and 1995, and is co-founder of Snowbush, a microelectronics company. He served as an Associate Editor for *IEEE Transactions on Circuits and Systems Part II* from 1993



to 1995 and for Part I from 1995 to 1997. Dr. Johns is an IEEE Fellow.

Neil Weste received a BSc, BE(Elec) and PhD from the University of Adelaide, Australia. He commenced working for Bell Labs in 1977, working on early VLSI design tools



(the MULGA suite). He taught at Duke and UNC, Chapel Hill, from 1981 to 1982 and was Vice President of Design & Systems at MCNC in North Carolina. In 1984 he joined Symbolics to lead an effort on the Ivory single chip Lisp machine. Following this in 1985, he co-founded TLW, a chip engineering firm. In 1995 he returned to Australia to join Macquarie University as Professor of Microelectronics. He co-founded Radiata Communications in 1997 (IEEE 802.11a chipsets), which was

acquired by Cisco Systems in 2001. He currently is employed by Cisco Systems Wireless Networking Business Unit in Sydney, Australia, as Director of Engineering. His interests are wireless networking, Systems-on-a-chip, analog, RF, and digital IC design, and technology incubation. Dr. Weste has been an elected member of the SSCS AdCom since 1999.

Takayasu Sakurai received his BS, MS, and PhD degrees in EE from the University of Tokyo, Japan, in 1976, 1978, and 1981, respectively. In 1981 he joined Toshiba Corporation, where he designed CMOS DRAM, SRAM, and BiCMOS ASICs. He also worked on interconnect delay and capacitance modeling, known as the Sakurai



model and the alpha power-law MOS model. From 1988 through 1990, he was a visiting researcher at UC, Berkeley, doing research in the field of VLSI CAD. In 1990 he returned to Toshiba, where he managed RISCs, media processors, and MPEG LSI designs. Since 1996 he has been a professor at the University of Tokyo, working on low-power and high-performance system LSI designs. He has published more than 250 technical papers and several books, and holds more than 50 patents. He served as a Conference Chair for the Symposium on VLSI Circuits, and has been a program committee member for ISSCC, CICC, DAC, ICCAD, FPGA workshop, ISLPED, ASPDAC, TAU, and other international conferences. His current research interests include ultra low-power design of VLSI systems, battery-less systems, system in a package, and high-speed interconnects, including signal integrity. ●

Call for Nominees for SSCS Administrative Committee Election

In accordance with its Constitution, the IEEE Solid-State Circuits Society invites members of our Society to nominate candidates for the Society's Administrative Committee (AdCom).

Nominees by Petition

Petition nominees will automatically be placed on the ballot provided:

- The nominee is presently a member of the IEEE Solid-State Circuits Society.
- The petition is supported by at least ten identifiable signatures of present members of the Society.
- The nominee is both aware of and agrees to the petition.
- The petition is received at the SSCS Executive Office by 1 May 2002.

Terms of Office

The term of office is three years beginning 1 January 2003.

AdCom members may be reelected to a second consecutive term.

The five nominees receiving the highest number of votes from the Society membership will be elected.

Scope

Elected AdCom members can expect to attend at least two yearly meetings. In addition, much of the Committee work is carried on by email, telephone, and fax throughout the year. The Solid-State Circuits Society currently sponsors *The Journal of Solid-State Circuits*, the International Solid-State Circuits Conference, the Custom Integrated Circuits Conference, the VLSI Circuits Symposium, and the Solid-

State Circuits and Technology Committee's workshops. In addition, the Society cosponsors or technically cosponsors a number of other conferences and meetings.

The AdCom has responsibility for the overseeing of these and other potential future technical activities within the Society's field of interest.

Mailing Petitions

All petitions should be accompanied by a personal photograph and a short biography (200 words or less), including the nominee's technical areas of interest. Petitions must be received by 1 May 2002. Petitions should be mailed to:

IEEE SSCS Executive Office
445 Hoes Lane
Piscataway, NJ 08855-1331 ●

Retrospective on the 2001 Symposium on VLSI Circuits

The 2001 Symposium on VLSI Circuits was held 14-16 June in Kyoto, Japan. The Symposium covered all aspects of transistor-level design including memories, multimedia networking, data transmission, and design optimization. This year there were 431 attendees from 16 countries. A record 76 papers were presented, chosen from 153 submissions. Particularly exciting this year was the unprecedented increase in papers presented by students from colleges and universities. Many of these papers were selected by the Session Chairs to be the highlighted papers for the Symposium. In spite of the recent difficult economic times, the Symposium has experienced increased attendance over each of the last three years. This, together with the surge of high quality university papers, is a very positive sign for the future.

Those attending the Symposium were afforded the opportunity to attend a memorable Short Course on low-power microprocessors, take part in a number of interactive rump sessions, and listen to presentations covering novel and leading-edge concepts in communications, memory, analog circuits, and display electronics. On the final night of the Symposium attendees received a taste of local culture with a demonstration, audience participation included, by the Gion Taiko group.

As is our annual tradition, the Symposium on VLSI Circuits is held in conjunction with the VLSI Technology Symposium. Having these two symposia together affords opportunities for engineers and scientists from many nations in technology and circuits/systems to interact. This year the interaction was highlighted by our joint rump session “Which features of an IC technology will benefit radio system on a chip?” The rump session succeeded in bringing together a broad range of expertise to discuss the main technology features required to minimize cost and power of hand-held devices in this potentially



Attendees at the VLSI Circuits Symposium receive instruction in traditional wireless communications from the Gion Taiko Group.

huge market. The rump sessions at the 2001 Symposium were found to be exciting and stimulating, as evidenced by the consistent high attendance throughout the evening.

The day prior to the Symposium, M. Matsui of Toshiba and Greg Taylor of Intel set the high standard for this year by organizing a very topical one-day Short Course on the “Physical design for low-power and high-performance microprocessor circuits.” Each presentation in this exciting course featured speakers, who are the leaders in their field, teaching others how to do what they do best. The course started off with J. Moench of AMD describing the “Interconnect design of Athlon™ microprocessors” and was followed by K. Ishibashi of Hitachi presenting “Substrate-bias techniques for SH4.” The afternoon started with C.T. Chung of IBM discussing “High-performance SOI digital design — from devices to circuits,” followed by H. Takahashi of Texas Instruments teaching about “Low-power and high-performance circuit design of general-purpose DSPs.” S. Miyano of Toshiba taught about “Embedded DRAM SOCs and its application for MPEG4 Codec LSIs,” and L.T. Clark of Intel punctuated this very successful Short Course with his presentation on “Circuit design of Xscale™ microprocessors.”

Each of the first two days of the Symposium started with invited talks. M. Ishikawa and T. Komuro of the University of Tokyo presented a paper on “Digital vision chips and high-speed vision systems,” while Chenming Hu of the University of California, Berkeley, summarized years of outstanding contribution to the industry in his talk on “BSIM model for circuits using advanced technologies.” On the following day, K. Yoneda et al. of Sanyo Electronics presented “Development trends of LTPS TFT LCDs for mobile applications.” Peter van Kessel of Texas Instruments followed with his presentation on “Electronics for DLPTM technology-based projection systems.” The latter quietly substituted his palm-sized projector for a 50-kg auditorium projector and, with a flair for theatrics, revealed this to the audience at the end of presentation.

The strong tradition of memory papers was highlighted in this year’s Symposium by papers addressing a broad cross section of technical issues. “A bit-line GND sense technique for low-voltage operation FeRAM” was presented by S. Kawashima et al. of Fujitsu. In addition, D. Takashima et al. of Toshiba reported their work on “A cell transistor scalable array architecture for high-density DRAMs.” Closing out the memory presentations was M.

Yamaoka et al. of Hitachi who reported their work on "A system LSI memory redundancy technique using an ie-flash (inverse-gate-electrode flash) programming circuit."

Low power at higher performance has been an emerging theme of the VLSI Circuits Symposium and this year we had a variety of strong contributions. "A sub-130nm conditional keeper technique" was reported by Ram Krishnamurthy et al. of Intel. S. Kim et al. of the University of Illinois, Urbana-Champaign, reported on "A low-swing clock double-edge triggered flip-flop." In addition, Ram Krishnamurthy et al. of Intel described their work on "A 0.13- μ m 6-GHz 256x32b leakage-tolerant register file." Explaining how to provide just enough power for the application, J.Kim and M. Horowitz of Stanford University presented "An efficient digital sliding controller for adaptive power supply regulation." Finally, the concepts of leakage current reduction were presented in "A 63- μ W standby-power microcontroller with on-chip hybrid regulator

scheme" by M. Hiraki et al. of Hitachi.

The future of wireless was well represented by three strong papers from the academic community.

"A 15-GHz wireless interconnect implemented in a 0.18- μ m CMOS technology using integrated transmitters, receivers, and antennas" was presented by B. A. Floyd et al. of the University of Florida. A paper by Y. Koo et al. of Seoul National University described "A fully-integrated CMOS frequency synthesizer with charge-averaging charge pump and dual-path loop filter for PCS- and cellular-CDMA wireless systems." Finally, S. Mahdavi and A. A. Abidi of UCLA reported their work on a "Fully integrated 2.2-mW CMOS front-end for a for a 900-MHz Zero-IF wireless receiver."

The strong tradition of high-quality analog papers in the Symposium was represented by a truly global collection of featured papers. "A 1.57-GHz fully integrated very low phase noise quadrature VCO" was reported by P. Vancorenland and M.

Steyaert of ESAT-MICAS, Belgium, and "An optimally coupled 5-GHz quadrature LC oscillator" was presented by P. van de Ven et al. of Phillips Research Laboratories and Eindhoven University of Technology. In the area of converters, A. Shabra and H.S. Lee of the Massachusetts Institute of Technology discussed their work on "A 12-bit mismatch shaped pipeline A/D converter." From Matsushita, T. Morie et al. reported "A 200-MHz 7th-order equiripple continuous-time filter by design of nonlinearity suppression in 0.25- μ m CMOS process." Rounding out this fine collection of analog papers was "A temperature-stable CMOS variable-gain amplifier with 80-dB linearly controlled gain range" by T. Yamaji et al. of Toshiba.

We hope you will join us this June in Honolulu, Hawaii, for the 2002 Symposium on VLSI Circuits so that you may experience all aspects of the Symposium. ●

David Scott

2002 Symposium on VLSI Circuits Chair

Chapters Update

I am very pleased to open this month's column by welcoming two new Chapters: the Bangalore, India, Chapter, under the leadership of Dr. Navakanta Bhat of the Indian Institute of Science, and the Waterloo, Canada, Chapter, chaired by Dr. Arokia Nathan of the University of Waterloo. Both chapters are joint with the Electron Devices Society.

Once again, I would like to congratulate the Seoul Chapter for receiving the 2001 SSCS Outstanding Chapter Award. Dr. Moon Key Lee's group has done a marvelous job of organizing high-quality Chapter activities over the last few years. The award will be presented formally at the Plenary Session of the ISSCC this coming February in San Francisco.

In August the AdCom of the SSCS reviewed and approved various Chapter subsidy requests that we received. Twenty-three Chapters applied for subsidies, for a total of

approximately \$18,000, and the checks have either gone out or will be going out shortly. I was very impressed by the scope and range of activities that were being proposed, which included the organization of workshops, courses, Distinguished Lectures, membership drives, Web development, and student awards.

Please feel free to submit a write-up on your Chapter activities to the SSCS newsletter. In this issue we are featuring the Novosibirsk, Siberia, Chapter which, under the leadership of founding Chair Dr. Boris Kapilevich, has seen tremendous growth over the last five years. Subsidies have played a key role in the success of the Chapter. Dr. Kapilevich has stepped down as Chapter Chair after a five-year tenure of remarkable activity, and I would like to

thank him as well as welcome his successor, Dr. Wjacheslav Shuvalov.

Another ISSCC Chapters' meeting and luncheon is scheduled for Wednesday, 6 February 2002 at 12 noon in San Francisco. I hope that many of the Chapter Chairs or Co-Chairs will be able to join us. As with previous years, you will have an opportunity to present some of your best Chapter practices. Also, an IEEE representative will be there to talk about some of the Institute's initiatives relating to Chapters. Of course,

3 Good Leads for Literature in
Solid-State Circuits
The 12-CD Album
ISSC Collection
• ISSCC articles from 1966 to 2000
• ISSCC abstracts from 1955 to 2000
www.shop.ieee.org search JC41066C

Chapters Update *continued*

we welcome your suggestions and comments on how we can further improve support.

Dr. Christer Svensson is currently heading the Distinguished Lecture (DL) program and he has been involved actively in expanding the number of talks and speakers. For more information take a look at the DL home page: www.sscs.org/dl. The DL program is a great resource for organizing seminars and inviting top-quality speakers.

Finally, please remember that if you are interested in founding a new Chapter or organizing a current Chapter, information is available on the SSCS Chapter page: www.sscs.org/chapter.htm.



Jan Van der Spiegel
Chapters Coordinator
jan@ee.upenn.edu

Novosibirsk Joint Chapter Changes Leadership

After five years of remarkable growth under the leadership of founding Chair Boris Kapilevich, Siberia State Academy of Telecomm and Informatics (SibSUTI), the Novosibirsk joint Chapter elected Wjacheslav Shuvalov, SibSUTI, as Chapter Chair at its annual meeting held 23 October 2001. Dr. Shuvalov is a high-level professional in the area of communications, having long-term experience in industry and in the academic field. He can be reached at shwp@neic.nsk.su.

The Novosibirsk Chapter was formed in May of 1996 during a very difficult period for local profession-

als, caused by new reforms carried out in the former Soviet Union. Understanding that the income of most individuals in the newly formed Chapter was very low, IEEE Societies provided financial support, including free subscriptions for IEEE publications. This helped the Novosibirsk Chapter consolidate high-tech specialists and create a real IEEE community. There were only two IEEE members in Novosibirsk before formation of the Chapter. Now, the Chapter boasts more than 60 members. About 40% of members are self-paying. The Chapter currently is affiliated with five Professional IEEE Societies: MTT, ED, CPMT, ComSoc, and SSC. As a result, the Chapter has grown spectacularly and has become the largest organization of its kind in the Siberia region.

Here are some of the remarkable Chapter initiatives of the last five years: International Conference on Actual Problems of Electronics and Instrumentations Engineering (APEIE '96, '98, '00), International Conference on Microwave Electronics: measurements, identifications, applications (MEMIA '97, '99, '01), International Korea-Russia Symposium (KORUS '99, '00, '01), International Conference on Modern Information Technologies (MIT '00), and regular regional conferences dedicated to Solid State Circuits, Electronics, Communications, and Components & Packaging. Most of these events have been accompanied by Conference Proceedings, which are distributed through the IEEE Book Broker program and are available worldwide through the IEEE online store: <http://shop.ieee.org>.

The Chapter has been involved



Dr. Wjacheslav Shuvalov of SibSUTI, formerly Vice Chair, takes over as the new Chair of this rapidly growing joint Chapter based in Novosibirsk, Siberia.

actively in the formation of other Chapters and Student Branches in the Siberia region, such as the ED and SSC Student Branch at Novosibirsk State Technical University. Three other Student Branch Chapters, each with a different Society focus, have been formed at different academic institutions. As a result, the total number of IEEE members including student members is about 150. With this core, the Novosibirsk Section anticipates the formation six other Chapters in Krasnojarsk and another Student Branch in the Siberia State University of Telecommunications & Informatics. Hence, the formation of a Siberia IEEE Section is now becoming a reality.

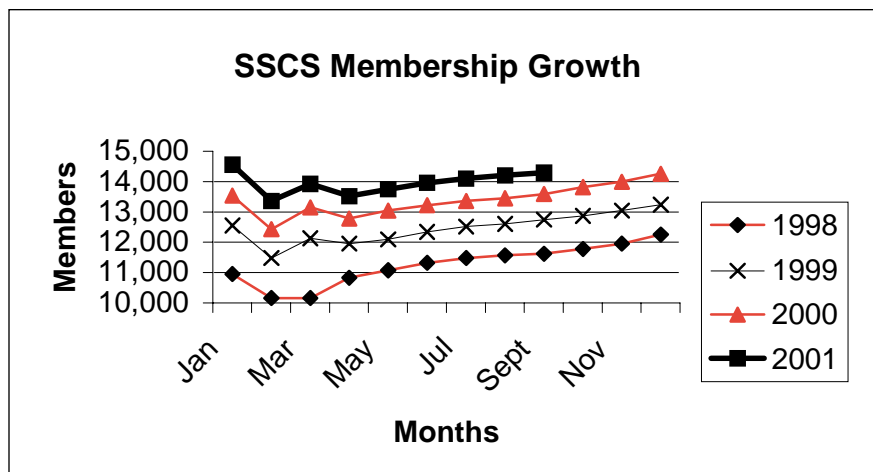
As Kapilevich stepped down he sent this message to each of the five IEEE Societies that support the Chapter: "I have appreciated very much the fruitful cooperation with each of you during my Chapter's Chair service and believe that you will share with all Novosibirsk's Chapter members our joint achievements in practical realization of the IEEE Globalization Project." ●

Boris Kapilevich
Past Chapter Chair
boris@sibnet.ru

Invest in Yourself: Remember to Renew

The best investment in a slow economy is yourself. Renew your membership in the IEEE Solid-State Circuits Society. An IEEE survey of engineers' salaries in 2001 showed solid-state circuits engineers are the highest paid of all engineering categories. And, if you agree that the articles in the *Journal of Solid-State Circuits* and the news in the quarterly newsletter are worthwhile, recommend membership to a friend.

SSCS membership has been growing at about 6% to 7% per year, among the best growth rates in IEEE Societies. Between January and February each year about 1,000 members in the United States let their memberships lapse. April is the



month that non-United States membership lapses are recorded. All year long former members reactivate and new members join for the first time. Lapsed members miss issues and

opportunities. If you forgot to renew you can do it online with a Web account at www.ieee.org/membership/renewal/. ●

Invest in a Colleague: Nominate an IEEE Fellow

An IEEE Fellow is a member of unusual distinction in the profession. This recognition is conferred only by invitation of the Board of Directors on a person of extraordinary qualifications and experience who has made important individual contributions to one or more of the IEEE fields of interest. No more than one-tenth of one percent of the total Institute membership may be advanced to Fellow grade in any given year.

A nominee must be a Senior Member of the Institute and must have been a member in any grade for at least five years prior to the year of election. Each nomination is evaluated by the relevant technical society or council, and all nominations are then rated and ranked by the 26-member IEEE Fellows Committee. Multiple reviewers produce a composite viewpoint that is used in recommending suitable candidates to the Board of Directors for election to Fellow grade.

The number of nominations evaluated by our Society is below that of other IEEE societies of comparable size. As a Society, we simply are not doing an adequate job of rec-

ognizing the very significant contributions our members have made to our profession. We must reverse this trend.

The Fellow nomination process is relatively straightforward but does require some forethought and planning. The Fellow nomination form is four pages long. It is not difficult to complete and should focus on the technical achievements of the nominated candidate. It is usually completed in collaboration with the nominee.

The deadline for receipt of the nomination form and reference letters is 15 March 2002. The nominator does not have to be an IEEE Fellow or even an IEEE member; self-nomination, however, is not allowed. A minimum of five and a maximum of eight references are required from current IEEE Fellows, who are listed alphabetically at the beginning of the IEEE Membership Directory.

If the nominee is not an IEEE Senior Member, the Senior Member application and its three supporting ref-

erences must be submitted no later than 4 February 2002. Senior Member forms and references can be emailed or completed online: Senior-member-forms@ieee.org; URL: www.ieee.org/organizations/rab/md/smforms.htm. Snail mail is also acceptable.

Fellow kits can be requested in hard-copy format (Fax: +1 732 981 9019) or downloaded from the Web (email: fellow-kit@ieee.org ; URL: www.ieee.org/about/awards/fellows/forms.htm). The Society welcomes suggestions of members who should be nominated for Fellow. ●

Richard C. Jaeger
Awards Chair
jaeger@eng.auburn.edu

3 Good Leads for Literature in Solid-State Circuits

2 The DVD Digital Archive

- JSSC articles from 1966 to 2000
- ISSCC articles from 1955 to 2000

www.shop.ieee.org search JD3755

Invest in the Profession: Make a Nomination for the Solid-State Circuits Award

“Awesome” is how young members see the pioneering breakthroughs that have given solid-state circuits the technical and economic impact it has today. How can so many engineers design million-transistor circuits with confidence and get products to market on time? What technical advances and what algorithms are almost invisibly intuitive in our thinking and software processes? How do we know where to start, where it is still too risky invest time, or what is too risky to tweak? If you can remember a decade or more ago when you dreamed about the work your team accomplishes today, you can remember the seminal ideas that allowed circuits to evolve a hundredfold. You could be a nominator for the IEEE Solid-State Circuits Technical Field Award—the Institute’s highest honor for outstanding contributions in our field.

Since the 1980s this award has reflected the progress of the technology. The history of the field is the textbook for tomorrow’s engineers. How is it that engineers can design faster, smaller, and denser circuitry every year? Look back, look around. Some of the ideas and authors are probably



on the *Solid-State Circuits Digital Archive* DVD. The Solid-State Circuits Technical Field Award consists of a bronze medal, a certificate, and a \$10,000 cash prize, and is presented at the ISSCC. It honors an individual, or team of up to three, for outstanding contributions in the field of solid-state circuits, as exemplified by enhancement to technology, benefit to society, and professional leadership. The nomination form is available to download online: <http://www.ieee.org/about/awards/noms/solidnom.htm>.

Guidelines, also available online, emphasize the importance of the nominee’s accomplishments, the quality of the nomination itself, and the quality of the supporting endorsement letters. The true merits of a candidate need to be conveyed through the nomination and endorsement paperwork. The deadline for receipt of nomination materials (including nomination form and the supporting letters) is 31 January 2002.

For further information, to coordinate your efforts with others, or to determine if a nomination is already in progress, please contact Dick Jaeger, the Chair of the SSSC Awards Committee, at jaeger@eng.auburn.edu. ●

Past Solid-State Circuits Award Recipients

2002

Chenming Hu

Taiwan Semiconductor Manufacturing Company

Hsin-Chu, Taiwan

Ping K. Ko

Authosis, Inc.

Quarry Bay, Hong Kong

“For BSIM3 modeling and development work”

2001

No award

2000

Robert H. Krambeck

Tandem Computers (Retired)

Cupertino, CA

Hung-Fai (Stephen) Law

Alaris, Inc.

Fremont, CA

“For pioneering the introduction and implementation of domino CMOS logic”

1999

Kensall D. Wise

University of Michigan

Ann Arbor, MI

“For pioneering contributions to the development of solid-state sensors, circuits, and integrated sensing systems”

1998

Nicky Chau-Chun Lu

Etron Technology Inc.

Hsinchu, Taiwan

“For pioneering contributions to high speed dynamic memory design and cell technology”

1997

Robert W. Brodersen

University of California

Berkeley, CA

“For contributions to the design of integrated circuits for signal processing systems”

1996

Rudy J. Van De Plassche

Philips Research Labs

Eindhoven, The Netherlands

“For pioneering contributions to the design of integrated circuits for data conversion”

1995

Lewis M. Terman

IBM - T. J. Watson Research Center

Yorktown Heights, NY

“For leadership in the field of MOS devices and circuits for semiconductor memories”

1994

Paul R. Gray

University of California

Berkeley, CA

“For contributions to analog integrated circuit design, especially for MOS switched capacitor circuits”

1993

Kiyoo Itoh

Hitachi, Ltd.

Tokyo, Japan

“For technical contributions to folded data-line circuits and the development of high-density dynamic RAMs”

1992

Barrie Gilbert

Analog Devices

Beaverton, OR

“For contributions to non-linear analog signal-processing circuits”

1991

Frank Wanlass

Standard Micro Systems

San Jose, CA

“For the invention of Complementary MOS (CMOS) Logic Circuitry”

1990

Toshiaki Masuhara

Hitachi, Ltd.

Tokyo, Japan

“For pioneering contributions to NMOS depletion-load circuits and the development of high-speed CMOS memories.”

1989

James D. Meindl

Georgia Institute of Technology

Atlanta, GA

“For contributions to solid-state circuits and solid-state circuit technology”

Find Out What's Happening: <http://whatsnew.ieee.org/>

Did you hear about the new IEEE Job Site with *IEEE eRecruiter™*, that connects technical job seekers with prospective employers? Users can create a personal profile, including desired salary, job location, and discipline. Jobs matching user profiles will be emailed to potential applicants, or users can search the entire site. Over 975 employers were registered on the site as of 5 October.

Did you hear about the newly released *Radio Frequency Circuit Design*, Vol. 1 that was published last year? Authors W. Alan Davis and Krishna Agarwal provide engineers with the technical resources to design and analyze RF circuit components. Focusing on circuits used

at the 800-MHz to 2-GHz range, this guide explores filters, impedance transformers, oscillators, class A amplifiers, and more.

Did you hear about *The ASIC Handbook*, written for project managers, team leaders, designers, and developers by Nigel Horspool and Peter Gorman? It explores the phases of an ASIC design project, including the techniques and methods for successful management. It covers design for reuse, improving the quality of initial designs and architectures, simulation, and verification, and other ways to convert



ideas into working prototypes.

Subscribers to *What's New@IEEE* in Circuits did. They receive a monthly email alert on new publications, industry news, conferences, and IEEE electronic services. An email issue highlights 10 quick picks per month, which link to online sites where the full story can be read. Last September alone, subscriptions jumped 40%.

The *What's New* program, with eleven titles, now has over 100,000 subscribers. The IEEE sent out a total of over 120,000 *What's New* email solicitations from IEEE President Joel Snyder in September. The result: almost 25,000 more subscriptions—a 31% increase.

The newsletters with the highest percentage increases in September:

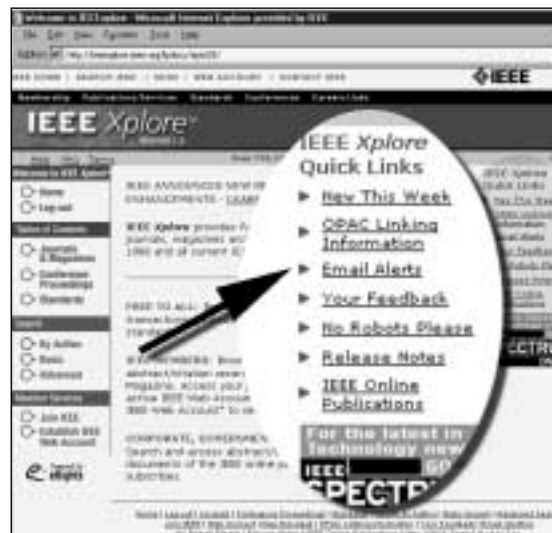
- Eye On Washington - 46%
- Circuits - 40%
- Communications - 39%
- Power - 38%

Journal Table of Contents Via Email

Get email alerts on the table of contents of any IEEE journal, transaction or magazine, whether you are a paid subscriber or not. In November 2001 IEEE *Xplore™* announced this new service. Members and nonmembers can use this service to find out about articles as soon as they are posted. Regular subscribers will be alerted to their next issue before it arrives through their postal service.

You choose the titles that you want to know about. Each email contains a direct link to the issue's latest table of contents. From the table of contents you will be able to jump to full abstracts of any article through your personal member log in or through your institutional library portal.

Conference Proceedings and Standards are not available for email alerts. Discontinuing the table of contents alert service is easily accomplished through the same form submission process. Access the IEEE *Xplore* homepage and look under the Quick Links listed on the right of the screen for email alerts.



SSCS EVENTS CALENDAR

Also posted on www.sscs.org/meetings

SSCS Sponsored Meetings

2002 SSCTC Workshop on Analog Telecom Access Circuits and Concepts

www.ieee.org/ssctc

3 February 2002

San Francisco Marriott Hotel, San Francisco, CA

See new registration contact below.

2002 ISSCC International Solid-State Circuits Conference

www.isscc.org

3-7 February 2002

San Francisco Marriott Hotel, San Francisco, CA

2002 ISSCC NEW REGISTRATION CONTACT:

Registrations since November 12 with Seminar Source are invalid. You MUST register with IEEE who will provide a confirmation. You are urged to register on line.

IEEE/CMS

ATTENTION: Ms. Christy Lankenau

445 Hoes Lane, Piscataway, NJ 08854 USA

Telephone: 1-800-810-4333 (within the U.S. only)

Direct Line: 1-732-981-3415

Fax: 1-732-465-6447

Email: ISSCC02reg@ieee.org

2002 CICC Custom Integrated Circuits Conference

www.bis.com/~cicc

12-15 May 2002

Caribe Royale Resort Suites, Orlando, FL

Paper deadline: past

Contact: Ms. Melissa Widerkehr, cicc@his.com

2002 Symposium on VLSI Circuits

www.vlsisymposium.org

13-15 June 2002

Hilton Hawaiian Village, Honolulu, HI

Deadline for receipt of summaries: 8 January 2002

Contact: Phyllis Mahoney, vlsi01@aol.com

or Business Center for Academic Societies Japan

vlsisymp@bcasj.or.jp

To maintain all your IEEE and SSCS subscriptions,
email address corrections to:
address-change@ieee.org

Technically Cosponsored Meetings

2002 Radio Frequency Integrated Circuits Symposium

www.rfic2002.org/

2-4 June 2002

Seattle, WA

Deadline for Papers in .doc format: past

See website for additional deadlines for other formats.

2002 ACM/IEEE Design Automation Conference

www.dac.com/

10-14 June 2002

New Orleans, LA

Paper Deadline: past

2002 Symposium on VLSI Technology

www.vlsisymposium.org

11-13 June 2002

Hilton Hawaiian Village, Honolulu, HI

Deadline for receipt of summaries: 8 January 2002

Contact: Phyllis Mahoney, vlsi01@aol.com

2002 European Solid-State Circuits Conference

ele.unipv.it/esscirc2002/index.html

24-26 September 2002

Florence, Italy

Deadline for Electronic Submission: 5 April 2002

IEEE SOLID-STATE CIRCUITS SOCIETY NEWSLETTER (ISSN 1098-4232) is published quarterly by the Solid-State Circuits Society of The Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. \$1 per member per year (included in society fee) for each member of the Solid-State Circuits Society. This newsletter is printed in the U.S.A. Periodicals postage paid at New York, NY and at additional mailing offices. **Postmaster:** Send address changes to IEEE Solid-State Circuits Society Newsletter, IEEE, 445 Hoes Lane, Piscataway, NJ 08855. ©2002 IEEE. Permission to copy without fee all or part of any material without a copyright notice is granted provided that the copies are not made or distributed for direct commercial advantage and the title of publication and its date appear on each copy. To copy material with a copyright notice requires specific permission. Please direct all inquiries or requests to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08855. Tel: +1 732 562 3966.



445 Hoes Lane
Piscataway, NJ 08855

