



Volume 5
Number 3
July 2000

SOLID-STATE CIRCUITS



IEEE Solid-State Circuits Society Quarterly Newsletter

Biomedical Electronics Workshop

Biomedical Electronics is the focus of the fall workshop organized by the Solid-State Circuits and Technology Committee (SSCTC) on 12-13 October in the Washington DC area. Held twice a year, these popular workshops focus on an emerging technology and limit attendance in order to promote good communication between the speakers and attendees.

Since the invention of integrated circuit technology in 1958, the con-

tributions of microelectronics to biomedicine and health care have been enormous. Many advanced diagnostic, therapeutic, and rehabilitative devices and systems would not have been possible without these contributions. One can simply not envision various imaging systems (computed tomography, magnetic resonance, and ultrasound), implantable therapeutic and prosthetic devices (cardiac pacemakers, implantable defibrillators, and neuromuscular stimulators), physiological monitors, and telemedicine without microelectronics and integrated circuits. This influence is growing at an increasing rate, partly due to the recent advances in microelectromechanical (MEMS)-based transducers and packaging technology, new and compact power sources (high-efficiency inductive powering and miniature batteries), CMOS low-power design, and wireless integrated circuits. These advances are enhancing the quality of care being delivered and can reduce health care costs. In addition, novel emerging technologies employing nanofabrication and its interface with biological components at the cellular and molecular level (nanobioelectronics) promise to revolutionize biomedicine in the 21st century.

The workshops are interactive meetings of experts, not tutorials or short courses. They are informal and no written presentation is required. Attendees are active in the field of the workshop. The speakers discuss the latest developments in



A single-channel implantable microstimulator for neuromuscular applications (developed at the University of Michigan) shown here in the bore of a 10-gauge hypodermic needle. Dr. Jeffrey Von Arx of Guidant Corporation will discuss this and other novel implantable microsystems at the 1^{1/2} day interactive workshop of experts on biomedical electronics scheduled for 12–13 October in the Washington, DC area.

their work, and there is significant time allocated for audience participation and discussion.

Topics discussed in the workshop will include circuit-oriented work in the following current and emerging technologies:

- Implantable electronics
- Power sources
- Biomedical transducers and their interface circuits
- Physiological monitoring and telemedicine
- Nanobioelectronics
- Microelectronics and VLSI in imaging
- Biotelemetry

Continued on next page →

IN this issue

<i>Biomedical Electronics Workshop</i>	1
<i>ISSCC 2001 Call for papers</i>	2
<i>Highlights of ISSCC 2000</i>	2
<i>IEEE Sensors Journal *New for 2001*</i>	5
<i>ESSCIRC 2000 Preview</i>	5
<i>Chapters Round-Up</i>	7
<i>Chapter Chairs Honored</i>	9
<i>Welcome New SSSC Senior Members</i> . . .	9
<i>AdCom Actions: February 2000</i>	10
<i>SSSC Members Honored as 2000 IEEE Fellows</i>	12
<i>Independent Short Courses</i>	18
<i>What's New @ IEEE in Circuits</i>	18
<i>Events Calendar</i>	20

ELECTRONIC SUBMISSION REQUIRED FOR ISSCC 2001 PAGE 2

The technical agenda is organized by Babak Ziaie of the University of Minnesota (email: ziaie@ece.umn.edu) with Jeffrey Von Arx of Guidant Corporation serving as co-organizer. The workshop will consist of approximately twenty 30-minute talks spread over 1.5 days, Thursday and Friday morning. Morning and afternoon coffee

breaks, in addition to a lunch and a reception on Thursday evening, will allow participants to interact.

How to Register

The Biomedical Electronics Workshop will be 12–13 October 2000 at the Key Bridge Marriott, Arlington, VA. Attendance is limited and pre-registration is required. The regis-

tration form is available at www.sscs.org/ssctc/applic00.htm. Inquiries on agenda, registration, and local arrangements should be addressed by fax or email to: Suzanne Demarie, Courtesy Associates, Fax: +1 202 973 8722; e-mail: demarie@courtesyassoc.com. ●



ISSCC 2001 Call for Papers Electronic Submission and Electronic Projection

For the first time the ISSCC 2001 will require electronic submission. A web site will be the interface. The system will ensure consistent listing and spelling of important presentation information, even before a sub-

mission is selected. After acceptance, the system will streamline the preparation of the Advance Program.

Also standardized are the Electronic Projection requirements for all sessions. The conference, is scheduled for 5–7 February 2001 in San Francisco, CA.

- Submitters should read carefully the new submission requirements at www.sscs.org/isscc/2001/cfp.htm.
- The deadline for submission is 6 September 2000.

Highlights of ISSCC 2000

In February, the International Solid-State Circuits Conference 2000 (ISSCC 2000) showcased the outstanding new designs and ideas for faster, smaller, cooler, cheaper chips that advance the state-of-the-art and simplify the work of end product designers. In November and December, watch for the *Journal of Solid-State Circuits*, special issue which will publish journal-length papers of selected ISSCC presentations.

Analog

This year's analog papers spanned four sessions: Nyquist-Rate Data Converters, Filters and Amplifiers, Oversampling Converters, and General Analog techniques. Behzad Razavi, the ISSCC 2000 Analog Subcommittee Chair, reported that each session included

record-breaking designs in CMOS and bipolar technologies.

In the first session, a 14-bit 100-MSample/s bipolar ADC and a 12-bit 65-MSample/s CMOS ADC are the fastest circuits reported to date for their respective resolutions. In the second session, a 10.7-MHz CMOS switched-capacitor filter is the first to achieve a well-defined, reproducible quality factor of 55, a critical feature for heterodyne RF receivers.

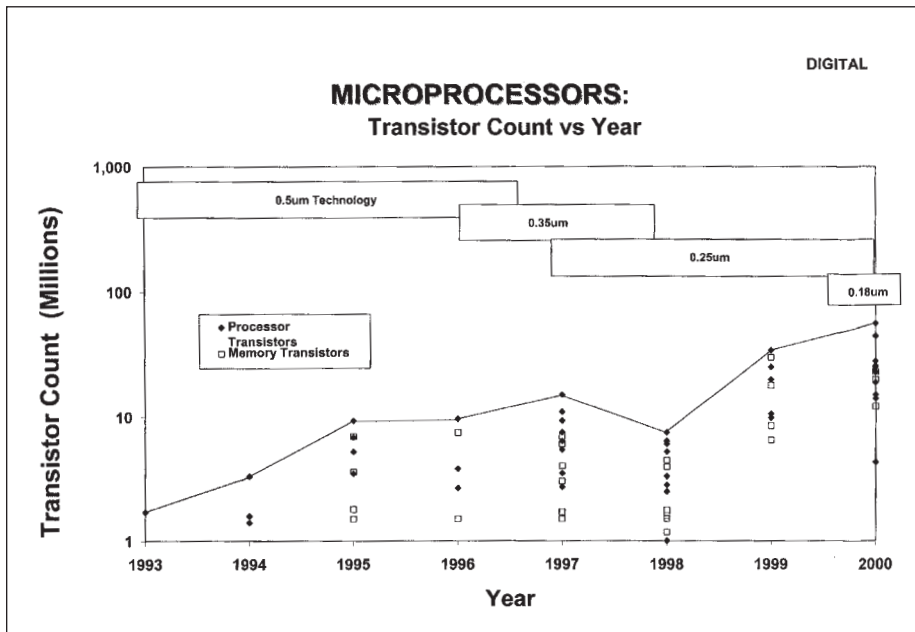
In the third analog session, two oversampling converters achieve an effective sampling rate of 2.5 MHz with a signal-to-noise ratio (SNR) of 90 dB and higher, providing low-cost solutions for DSL applications. A multibit converter providing 120 dB SNR is also reported. In the fourth session, a 6-bit 800-MSample/s ADC, targeting

disk drive electronics, achieves the highest conversion rate at this resolution in CMOS technology.

Communications

CMOS designs continue to dominate research presented at the ISSCC 2000 because of its usefulness for wideband wireless communications and its key role in creating low-cost portable broadband communication devices.

Paper 8.1 reported the first DECT phone-on-a-chip. Digital self-calibration and offset cancelation techniques solved DC offset issues common in Zero-IF circuits. The chip includes a high level of digital processing within a radio transceiver operating at 1.9 GHz. The chip boasts complete integration except for the power amplifier and antenna switch.



A blinding 16.8 GHz in CMOS for a frequency divider was shown in Paper 12.1. This is a 3x speed improvement over previously reported 1.8-V CMOS dividers, while dissipating just 3 mW. The design used a new frequency divider topology that made use of mutually coupled flip-flops to achieve a low-cost device.

The industry's first complete analog front-end for HDSL2 was introduced at the conference. Digital Subscriber Line (DSL) technology offers a competitive alternative to broadband access for businesses and homes by using the installed base of twisted-pair telephone wiring. Although HDSL is the current choice for T1 replacement for business use, it is a proprietary standard that is currently hampering the interoperability of equipment from different vendors. Moreover, HDSL requires two copper pairs. Presently, HDSL2 overcomes these two problems by standardizing high-bit rate data delivery over a single copper pair at T1 speeds of 1.544 Mbps. This IC, [Paper 18.1], accommodates the extremely high dynamic range and peak-to-RMS requirement of HDSL2 created by the overlapped transmission of the upstream and downstream data.

Gigabit Internet backbone com-

munications were described in two papers on SONET implementation. Paper 3.2 described a fully integrated receiver for SONET OC192 (10 Gb/s) contributing to higher-speed Internet service while achieving cost reduction. Another paper, 3.6, demonstrated clear progress towards integrated solutions with their chip-set for SONET OC768 (40 Gb/s).

Digital

Ian Young, Digital Subcommittee Chair, saw dramatic improvement in microprocessor performance this year over previous years, both in highest frequency clock rates reported and in the emergence of several brand-new microprocessor designs based on new architectural concepts. The 1-GHz barrier was crossed by no fewer than three microprocessors introduced at the conference. [Papers 5.1, 5.4, 5.7] Four of the microprocessors used the latest 0.18- μ m technology that enables twice the number of devices per unit area, each operating faster and consuming less power per operation. [Papers 5.1, 5.2, 5.3, 5.7] Of those, one, a GHz IA 32 Microprocessor [Paper 5.7] used aluminum interconnect to simplify the manufacturing process at the cost of added design complexity.

Two papers described the use of more than one type of n channel and p channel transistor threshold voltage on the same chip, allowing for the optimization of fast but hard to turn off transistors versus regular devices. In an IBM processor [Paper 5.6] and in an Hitachi processor [Paper 25.3], designers exploited the "lower-threshold" faster circuits in some systems on the chip, while still producing most transistors as the more controllable "higher-threshold" type. Paper 25.6 demonstrated use of a completely different method of modulating threshold voltage by dynamically adjusting the substrate bias to select speed and power.

New levels of chip integration were demonstrated in Papers 25.4 and 25.5, which include 17 and 4 independent processing units, respectively. Each of these on-chip processor units operates on its own instruction stream, greatly expanding the performance and flexibility of the chip. Similarly, to increase instruction-level parallelism in the traditional single-instruction stream processors, a doubling of transistors was used to increase the instruction per cycle. Paper 25.7 introduced the design of the much-anticipated IA 64 architecture, which makes use of Very-Long-Instruction Word (VLIW) concepts and advanced compiler technology to extract more performance from each instruction. The new SPARC processor presented in Papers 25.1 and 25.2 is able to execute up to seven instructions per clock versus four in the previous generation.

Self-adjusting clock distribution is a key technology for large gigahertz-class processors and digital ICs. Two papers present innovative approaches that minimize or eliminate the amount of interconnect required by using many DLLs or PLLs to locally generate the clocks needed in each region of the chip

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and to provide global synchronization. Paper 10.5 described an array of PLLs used in a distributed-clock network. Paper 10.6 described clock generation and distribution in the new IA-64 microprocessor.

Imager and MEMS

Dennis L. Polla, subcommittee chair, highlighted new imaging techniques based on CMOS and CCD technologies. The CMOS contributions focused on innovative methods for reducing fixed-pattern noise (FPN), increased frame rate, and reduced power consumption. Paper 6.1 used a hole-accumulation-diode sensing approach to reduce FPN. Dark currents of 370 pA/cm² were characterized at room temperature. Another FPN reduction technique in Paper 6.3 was implemented in the form of a 256 x 256-CMOS passive pixel imager with a differential architecture and correlated double-sampling output. This approach eliminated blooming effects often found in passive pixel approaches and demonstrated 0.1% pixel-to-pixel and 0.4% column-to-column FPN.

Paper 11.7 presented an embeddable low-power SIMD processor. The imager showed a new approach for future digital imaging system requirements of real-time image processing and real-time video compression. A prototype processor with 9.6- μ m-pixel pitch was realized in a 0.6- μ m, three-layer metal CMOS technology and showed 20-mW peak power consumption at 25 MHz and 2.5 V.

A variety of integrated sensors based on MEMS technologies were presented. A miniaturized ultrasound range finder microsystem based on thermally excited silicon

membrane transducers and a standard 0.8- μ m CMOS technology was presented in Paper 11.1.

A single-chip wireless pressure sensor provided an excellent demonstration of MEMS wireless power and data transmission up to distances of 1 m in Paper 11.4.

Memory

T. S. Jung, the session chair on DRAM, reports that DRAM designers are exploring two avenues for increased performance: embedding portions of DRAM onto logic devices and using high-speed synchronous interface to stream data on and off stand-alone memory devices.

This year, designers of the embedded DRAMs, have optimized the cycle and access time to match the applications, employing pipelining to achieve clock speeds of up to 1 GHz and an access time <4 ns. [papers 24.1, 24.2, 24.3, 24.4]

For discrete DRAMs, higher frequencies and cost reduction are the focus. Area-efficient DLL and cancellation of system skews are employed to achieve optimal re-timing of received and transmitted data [Papers 24.6, 24.7]. Cost improvements are achieved, both by more efficient core organizations and use of packaged-part tuning techniques that allow more devices to meet the tighter I/O timing specifications required in high-bandwidth interfaces [Paper 24.8].

Signal Processing

Steve Molloy and Bernard Shung selected these highlights from the signal processing sessions.

Reporting energy levels between 50 and 100 MIPS/mW, about eight times lower than conventional DSP processors, Paper 4.1 described a flexible implementation of base-band wireless functions integrated

four programmable processing elements and a global resource controller connected to a high-performance split-transaction bus. This multiprocessor DSP chip achieves 1.6 billion 16-b MAC operations per second.

Paper 14.1 presented the first fully integrated audio/video/systems MPEG-4 simple profile codec. Three RISC processors and required memory are included in 117 mm², implemented in 0.25- μ m CMOS.

A complete IP phone solution from audio samples to TCP/IP packetized data was presented in Paper 14.4. The terminal processor integrates a 32-bit RISC CPU, two 10/100 Base-T MACs and 2 Mb of SRAM.

Technology Directions

John Cressler, Chair of the Technology Directions Subcommittee, highlighted the following papers from sessions on low-temperature circuits and diagnostic techniques for microprocessors, emerging memory and device technologies, and high-frequency wireless.

Chip cooling will drive the next increment in microprocessor performance. 0.1- μ m CMOS conventional and SOI digital circuits optimized for sub-ambient temperature operation can achieve as much as a 3.3% speed improvement per 10°C decrease in temperature. Moreover, copper interconnect improves by 3.6% per 10°C decrease in temperature. Backside thin-film thermoelectric cooling will allow migration of sub-ambient operation from server applications to PCs [Papers 13.1, 13.2]

New optical diagnostic tools allow noninvasive debugging of critical paths and verification of timing models for microprocessors. Backside optical probes developed in Paper 13.4 have a spatial resolution approaching that of a single

Numbers in brackets refer to the paper numbers in the published proceedings of the conference. *The Digest of the ISSCC* is available as a soft-cover volume. The ISSCC 2000 CD-ROM version also contains the *Slide Supplement* which has the slides of each presentation as well as the *Digest of Technical Papers of the 1999 Symposium on VLSI Circuits*. Order online at the IEEE store: shop.ieee.org/store/. Key in ISSCC in the form blank on the Web page and click on the Search button.

transistor and provide 50-ps resolution timing analysis of an operating 0.18- μm microprocessor. In paper 13.5 backside picosecond image circuit analysis identifies cycle-time-limiting conditions. This analysis was fed back to hardware simulation for model tuning and improved manufacturing models.

For breakthroughs in memory technology, MEMS technology may be the key for disk storage density,

and magnetic-junction RAM may be the key for fast, low-power non-volatile memory. Paper 7.1 reports on a very-large-scale nano-mechanical system that impresses data on the surface of a polymer, with a demonstrated density of 200 Gb/in². Average read access-time is comparable to today's hard disks, but at lower power levels. Papers 7.2 and 7.3 rely on arrays of magnetic tunnel junctions (MTJ), written by passing

data-dependent currents through orthogonal conductors and read by discriminating between the different resistances induced by the low magnetic polarization states of the MTJs. The authors differed in their approaches to sensing the two states, with an interesting trade-off between the area required to store a bit and circuit sensitivity to process variations. The high voltages required to write Flash memory are avoided. ●

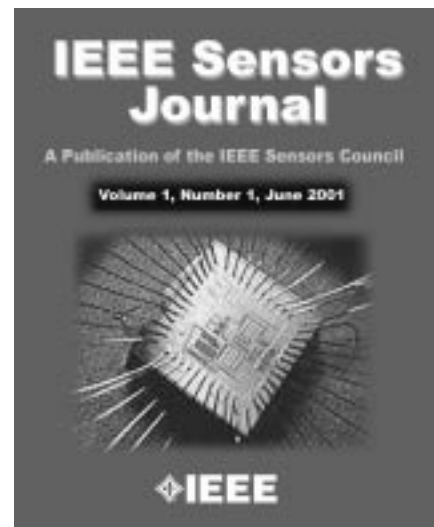
IEEE Sensors Journal *NEW for 2001*

The deadline for submissions to the inaugural issue of the *IEEE Sensors Journal* is 1 September 2000. The SSCS is a member of the IEEE Sensors Council, created last year to publish this *Journal*. The Call for Papers and other relevant information can be found on the Sensors Council Web site: www.ieee.org/sensors. Sensor researchers and users are invited to submit papers and help make the *IEEE Sensors Journal* the leading sensor publication in the world. Papers on sensor applications are of special interest to the *Journal*. The *IEEE Sensors Journal* will begin publication June 2001. The first issue is to consist of a collection of review papers covering a wide range of sensor technologies

The *IEEE Sensors Journal* covers the theory, design, fabrication, manufacturing, and application of devices for sensing and transducing

physical, chemical, and biological phenomena. With an emphasis on the application of sensors technology, this publication is sure to appeal to a wide audience of engineers. Focusing on the electronics and physics aspects of sensors and integrated sensor-actuators, the *IEEE Sensors Journal* will cover the numerous sensor technologies spanned by the IEEE as well as emerging sensor technologies.

The IEEE established the Sensors Council in 1999 for the purpose of creating a focus for the sensor activities of IEEE Societies and for starting a high-quality, affordable journal. The Council has 26 member Societies including the SSCS, with a combined membership of 260,000. The major competing journal costs \$5,200 per year. The *IEEE Sensors Journal* subscription price will be \$19 per year for IEEE members. The nonmember (institutional)



price will be \$395 per year. Published bimonthly, beginning with the June 2001 issue, the *IEEE Sensors Journal* will be a quality, peer-reviewed publication. Members may subscribe to this new *Journal* when they renew their membership and subscriptions this fall. ●

ESSCIRC 2000 Preview

The 26th European Solid-State Circuits Conference (ESSIRC) will take place 19-21 September in Stockholm, Sweden. ESSCIRC is an annual international circuits conference held in Europe. The conference rotates

among different European countries and is a true international event, with attendees and contributors from Europe, North America, and Asia. The organizational committee is chaired by Professor Hannu Tenhunen with Professor

ESSCIRC 2000



KUNGL. TEKNISKA HÖGSKOLAN

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Yrjö Neuvo, Nokia Mobile Phones, Finland will delivery the keynote speech, "Future in wireless," at ESSCIRC 2000 19 September, Stockholm.

Mikael Östling as cochair. The technical committee is chaired by Professor Kari Halonen with Professor Christer Svensson as cochair. Conference secretary is Zandra Lundberg, and Elena Dubrova is responsible for the local arrangements.

ESSCIRC addresses all aspects of solid-state circuits. There will be contributions in the areas of analog, digital, and mixed analog-digital solid-state circuits with applications in such areas as communications, computers, and sensors. Important contemporary topics are covered in eight invited papers in plenary sessions. These papers are listed below. Contributed papers are presented in three parallel sessions and as poster presentations. This year we

received a record 231 submissions, suggesting a very high quality conference! The conference usually features about 60 regular papers and 40 poster presentations, but due to the increased number of submissions this year, the number of presentations may be increased.

In connection with ESSCIRC 2000, four workshops have been organized. Each workshop has four to six distinguished speakers from the international scene. The day before the start of the conference, Monday, 18 September, there will be two workshops, Design Techniques for Mobile Equipments and CAD for Mixed Analog-Digital and RF ICs: The Current State of Art. The day following the conference's conclu-

The Venue

The conference will be held in Kista, in the north part of Stockholm. Stockholm, the capital of Sweden, is a very beautiful city, located on the waters of Mälaren and the Baltic Sea. The city offers attractive sights and cultural events. The conference evening program will give an impression of the beauty of Stockholm and its attractions. We will have a reception at the Stockholm City Hall (the traditional place for the Nobel Prize dinner) and the Conference Banquet in the Wasa Museum (which houses the recovered seventeenth-century ship found in Stockholm harbor). Kista is one of the most dynamically expanding regions in Europe in the field of mobile communications and is rapidly developing as one of the leading science parks in the world. Most major electronics companies in Sweden have either their head office or their branch office in Kista, employing about 25,000 people from the area. The Royal Institute of Technology (KTH) has recently established a new faculty of Information Technology in Kista. The premises of KTH will host the conference.

Highlights of the Conference

Invited papers:

- "Future in wireless," keynote speech, by Yrjö Neuvo, Nokia Mobile Phones, Finland*
- "Bluetooth: From antenna to silicon," by Jaap Hartsen, Ericsson Radio Systems, The Netherlands*
- "SOI CMOS circuit design exposed—another dirty tricks campaign?" by William Redman-White, Philips Semiconductors, U.K., and Kerry Bernstein, IBM Essex Junction*
- "Software-radio base stations, a challenge for analog IC-design," by Arne Rydin, Ericsson Radio Systems, Sweden*
- "VDSL, from concept to chips," by Paul Spruyt, Alcatel, Belgium*
- "Future trends in automotive electronics, sensors and communications systems," by Karl-Thomas Neumann, Volkswagen AG, Germany*
- "3-D ICs: Motivation, performance analysis, and technology," by Krishna Saraswat, Stanford University, Stanford, CA*

Workshops:

- Design Techniques for Mobile Equipments, organized by Philippe Garcin, ST Microelectronics, France*
- CAD for Mixed Analog-Digital and RF IC's: The Current State of Art, organized by George Gielen, Katholieke Universiteit, Leuven, Belgium*
- RF Circuits, organized by Ton Wagemans, Philips RF Business Development Center, U.S.A., and Christer Svensson, Linköping University, Sweden*
- Systemetic Analog Design: Hope or Hype, organized by Peter Jores, Robert Bosch GmbH, Germany*

sion, Friday, 22 September, two other workshops will be held: RF Circuits and Systemetic Analog Design: Hope or Hype.

We welcome you to attend ESSCIRC 2000. For more informa-

tion, visit the ESSCIRC Web site at www.esscirc.org or contact the conference secretary, Zandra Lundberg (Tel: +46 8 7521348, fax: +46 8 7527850, email: zandra@ele.kth.se). ●



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Chapters Round-Up

Chapters Newsletter July 2000

I am pleased to see that our current Chapters are very active in organizing activities for the benefit of their membership. A sampling of the activities of some of the Chapters is given below. I would like to congratulate the Dallas Chapter for its successful hosting of two SSCS Distinguished Lecturers, the Ireland Chapter for its undergraduate motivational design seminar, and the Iran Chapter for the organization of the IEEE International Millennium Seminar on Electrical Engineering in Tehran in March. If you would like your chapter activities to be included, please send a description to the Executive Office of the SSCS at sscs@ieee.org. We would be glad to publish them in the next newsletter.

I would also like to remind the Chapter Chairs that requests for subsidies are due 21 July 2000. All Chapters are eligible for a subsidy of up to \$1,000 to be used for activities that support Chapter operations, such as membership promotion, lectures, workshops, local newsletters, Web development, and so on. Details of how to apply can be found on the SSCS Chapters homepage: www.sscs.org/info/society/chapter.htm.

As always, the Society is interested in establishing chapters in sections where no chapter is currently present. If you are interested in forming a chapter or would like to explore formation, please

contact the Executive Office or myself. We would be glad to provide you with information on how to get started with forming a new or joint chapter.



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Dallas Chapter *Chair: Paul Yu*

Dallas Hosts Two SSCS Distinguished Lecturers

This past winter, the Dallas Chapter made good use of the Solid-State Circuits Distinguished Lecturer program by hosting two lecturers for their monthly meetings. In February, Professor Willy Sansen of Katholieke University of Leuven, Belgium spoke on Compensation Techniques, Feedforward and Settling Time in Opamps. In March, Professor Tom Lee of Stanford University, Stanford, CA, another SSCS Distinguished Lecturer, spoke about CMOS RF. Both of these presentations attracted excellent attendance.

Tom Lee Lecture on CMOS RF: Cheesy, but Tasty and Nutritious

To many, CMOS RF seems an absurd idea, almost an oxymoron. Compared with bipolars, CMOS has notoriously inferior gm/I and terri-

ble 1/f noise. Compared with GaAs, the lossiness of silicon substrates degrades the Q of inductors. Compounding these deficiencies is the somewhat primitive state of CMOS models (particularly with respect to broadband noise) in the RF regime. Nevertheless, CMOS has a surprising number of compensating attributes. The continuing tremendous investment in CMOS technology has kept Moore's law in effect longer than many had predicted. Devices with peak ft values in excess of 40 GHz are now in volume production, with 60 GHz not far behind. Both power gain and noise figure improve constantly as a result. At the same time, short channel effects result in a substantially constant gm over a reasonable range of gate voltages, leading to excellent linearity. Even though gm/I remains pathetic relative to bipolars, the dynamic range per current is about the same (perhaps better), and the latter is arguably more important for the front-end RF circuits that control most of a receiver's critical characteristics.

The number of interconnect layers keeps growing as well, and this trend has helped buy back some of the deficit in inductor performance. Improved analytical models show that substrate loss effects grow as the cube of the inductor diameter, leading to optimum inductors that are considerably smaller than is common practice in GaAs. Newly

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developed simple, but highly accurate, formulas for inductance also facilitate optimizations. Varactors with Q-f products of 200 GHz have also been realized using accumulation-mode structures that can be built in ordinary processes.

A new understanding of phase noise has also shown that device 1/f noise can be made much less important than was once believed, allowing a fully integrated CMOS VCO to achieve a -121-dBc/Hz phase noise at a 600-kHz offset from a 1.8-GHz carrier on 6 mW of power.

These recent advances were discussed along with how they enabled a single-chip GPS receiver in 0.5- μ m CMOS and a 5-GHz HIPERLAN transceiver in 0.25- μ m CMOS. To show that the fundamental limits lie far in the future, a 23-GHz distributed amplifier and 17-GHz oscillator in 0.18- μ m technology, as well as the characteristics of interconnect up to 50 GHz, were also described briefly.

Ireland Chapter

Chair: Peter Kennedy

Motivating Students Toward Circuit Design

Ireland's Microelectronics Industry Development Association (MIDAS) has identified a strong national demand for circuit designers. How can we convince more electrical engineering students to choose the field of circuit design? In an attempt to answer this need, the SSCS Ireland Chapter and Analog Devices jointly hosted a motivational design seminar for seniors on 2 March at the University College in Dublin. The seminar, entitled CMOS Op Amp Design, was lead by Dennis Dempsey. Analog Devices sponsored the event.

Sharif University, Iran Student Chapter

Behnam Analui

Chair: Ali Reza Motieifar

Iran Student Chapter Sponsors Lectures

To commemorate the new millennium, review past achievements, and forecast future trends in different electronic engineering fields, the IEEE Student Branch at Sharif University of Technology, Tehran, Iran, successfully organized the IEEE International Millennium Seminar on Electrical Engineering on 1-3 March 2000. Several international lecturers were invited to cover various branches of electrical engineering in their talks. The Solid-State Circuits Society Student Chap-

ter of Iran sponsored eight invited lectures and three short courses on topics listed in the following table.

Turnout at these events was excellent, with more than 200 students, faculty members, and industry professionals in attendance. The SSCS Student Chapter in Iran, supported by IEEE Student Branches at Sharif University of Technology and the University of Tehran, is potentially the largest Student Chapter in the Middle East. Growth in the student branch is being propelled by support from the IEEE Iran Section and some newly

Lecture Topic	Lecturer
"RF CMOS circuit design"	Professor Asad A. Abidi, University of California at Los Angeles; IEEE Distinguished Lecturer
"Low power design: Methodologies & techniques"	Professor Massoud Pedram, University of Southern California
"HDLs in digital system design process"	Professor Zainalabedin Navabi Shirazi, University of Tehran
"New directions in communications hardware in the 21st century"	Professor Ali Hajimiri, California Institute of Technology
"Fundamental challenges in VLSI CAD"	Professor Majid Sarrafzadeh, Northwestern University
"Future developments and new directions in design and applications of FPGAs"	Professor Seyyed Mehdi Fakhraie University of Tehran
"Testability of digital circuits"	Professor Shaahin Hessabi, Sharif University of Technology
"Mainstreaming SOI CMOS technology"	Dr. Ghavam Ghavami Shahidi, IBM Research Division

Short Course Topic	Teacher(s)
"Fundamentals of RF circuit design"	Professor Asad A. Abidi, University of California at Los Angeles; IEEE Distinguished Lecturer
"Research and industrial directions in VLSI design CAD"	Professor Majid Sarrafzadeh, Northwestern University and Professor Massoud Pedram, University of Southern California
"New DRAM technology"	Dr. Hassan Fallah-Adl, Intel Corporation

Seminar at Sharif University of Technology, Tehran

established companies active in solid-state circuits.

The Student Chapter has also developed a series of workshops dealing with various topics of interest to solid-state circuit design. The first two-day workshop, sponsored by Emad Semicon Co., was held 13-14 March 2000. More than 20 graduate students, faculty members, and invited guests, including Professor Ali Hajimiri from the California Institute of Technology, presented and discussed state-of-the-art achievements in several topics of rf analog circuits. Topics discussed included: "Power amplifiers," "Wireless LAN," "New LNA/Mixer," "Substrate noise and coupling," "Different synthesizers," "Frequency dividers," "Mixers

noise analysis," "IC identification," "Smart radio, and Oscillator phase noise." Follow-up discussions and active group participation provided many opportunities for all attendees to learn new information. Because this event was such a success, the next workshop is planned for May 2000. This workshop will focus on data converters, and various topics dealing with mixed signal circuits will be discussed.

ED/SSC University of Nis, Yugoslavia Student Branch Chapter
Aleksandar Jaksic, Chapter Chair

New SSCS Joint Student Chapter
In April 2000, our Student Branch Chapter was expanded to include

the Solid-State Circuits Society as a sponsor, in addition to the Electron Devices Society. The expansion was the result of a promotional campaign among students at our university to increase their interest in IEEE activities. This membership campaign was jointly conducted by high-grade IEEE members and Student Branch Chapter volunteers. Students were invited to presentations on IEEE mission and goals as well as the benefits of IEEE student membership. We would particularly like to mention all the help and support offered to our expansion by the very active Yugoslavia ED/SSC Chapter.

Activities of the ED/SSC Student Branch Chapter also consisted of successful educational and technical meetings with video presentations. The video presentation included: New Generation TCAD, a short course from the 1997 IEDM conference; Careers for Electrical Engineers and Computer Scientists; and Engineering and Technology Opportunities for All. Several interesting social events were also organized, including parties and picnics. The Student Branch Chapter members have also been helping to organize the MIEL 2000 conference in Nis 14-17 May 2000.

The Nis Chapter has ambitious plans for future activities. More meetings with video presentations will be held. We are organizing a lecture with one of the EDS or SSCS Distinguished Lecturers later this year. We are also organizing a project and applying for funds to provide our Student Branch Chapter with the appropriate room and computer access to IEEE electronic products, because, unfortunately, most Chapter members still don't have access to the Internet. The room will include a small library with a subscription to the Student Branch Magazine Package containing 33 IEEE magazines. For more information, please contact Chapter Chair, Aleksandar Jaksic at ajaksic@ieee.org. ●

Chapter Chairs Honored



Two SSCS Chapters are honoring their past Chairs this summer. At the June meeting of the Baltimore Chapter, Anna Roesch, the current Chair of the Chapter, thanked 1998-1999 Chair Paul Potyraj for forming the Chapter and presented him with the IEEE pin for past Chapter Chair. Palaksha Setty, the new Chair of the SSCS Santa Clara Chapter, will be presenting pins this September to honor all three of Santa Clara's past Chairs, founder Jonathan David, John F. Merrill, and outgoing Chair Jess Chen. Chapter chairs organize and publicize local programs and guest speakers. Other SSCS Chapters interested in honoring past or outgoing Chairs please contact Cathleen Macor at the Society's Executive Office: c.macor@ieee.org.

Welcome New SSCS Senior Members:

Rod Burt	John G. Kenney
Harold W. Carter	Yong-Bin Kim
T. J. Cumins	Huainan Ma
Nabil Derbel	Alberto Palacios-Pawlovsk
J. F. Duque-Carrillo	Alison J. Payne
Boaz Eitan	Leonard R. Rockett
Brian L. Evans	Maher M. Sarraj
John W. Fattarusio	Bertram E. Shi
Chris N. Hinds	Moise N. Solomon
David A. Hostetler	Ross E. Tegatz
Shoji Kawahito	Sorin Vaduva

Congratulations!

AdCom Actions: February 2000

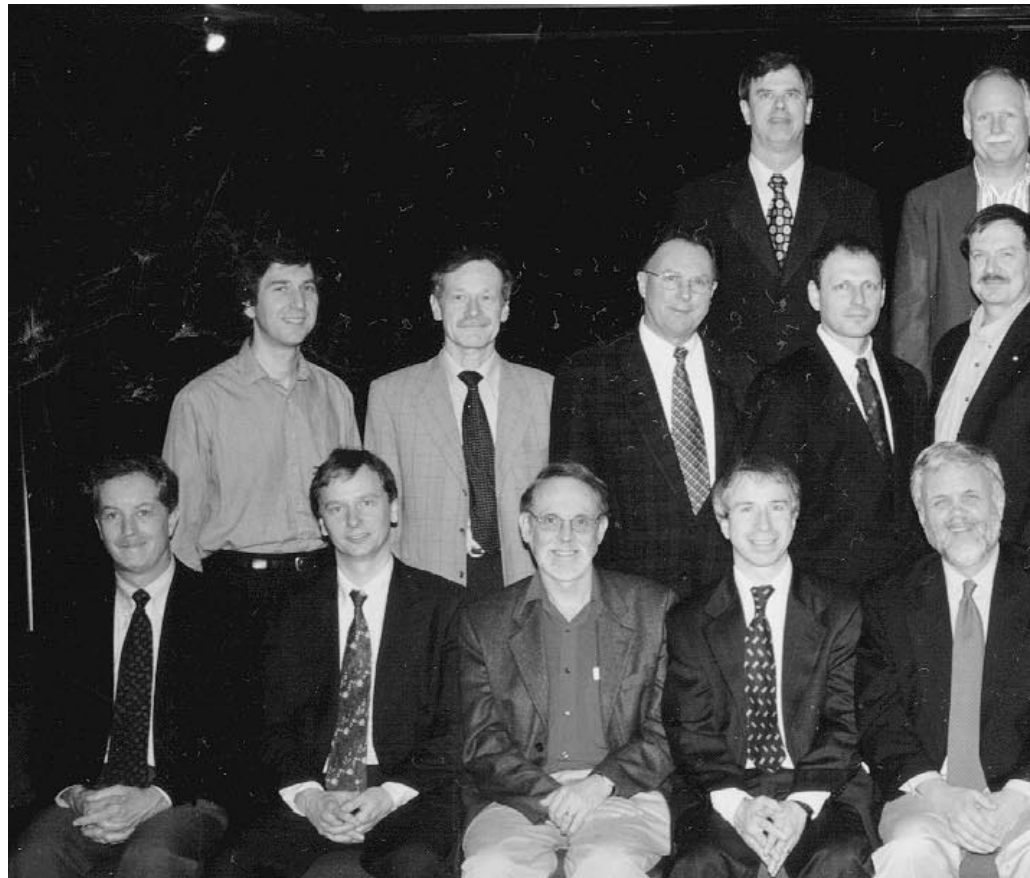
More Chapters and more members continue to characterize the rapidly expanding IEEE Solid-State Circuits Society, it was reported to the Administrative Committee (AdCom) on 6 February. All 22 voting members of the AdCom along with more than a dozen other Society leaders met the day before the ISSCC in San Francisco. Chapters have expanded from 20 to 30 in 6 months, while membership is now over 13,000 from a start of 7,000 just four years ago and is growing at 9% annually. In addition, there were status reports on conferences and workshops, the JSSC, and many projects that are making more Society intellectual property available electronically. Full minutes of the meeting, along with background attachments and presentations, are available at: www.sscs.org/info/minutes.

Outstanding Chapter of the Year Award

The AdCom has funded a new SSCS Outstanding Chapter Award to be given annually to an SSCS Chapter that has shown consistent, outstanding leadership and initiative in organizing activities. The criteria for selection will be based on:

- the quality and quantity of activities and programs sponsored by the Chapter
- the delivery of practical benefits for local Chapter members
- demonstrations of successful outreach programs to the professional community
- growth of Chapter membership

All Chapters were notified this spring about the award and its 1 July 2000 application deadline for the first year. The AdCom will decide on the outstanding Chapter during their 27 August 2000 meeting. The \$1,000 award is for chapter activities, and a Certificate of Recognition for display will also be presented during the week of the ISSCC, February 2001. More infor-



The SSCS AdCom met preceding the ISSCC. Seated I-r: John Corcoran, Gerhard Fettweis, Christ Charlie Sodini (Vice-President), T. R. Viswanathan. Standing I-r: Mark Horowitz, Willy Sansen, R. Baggio Bampi, Anantha Chandrakasan. Top I-r: Kevin O'Conner, Dick Jaeger, Chris Mangelsdorf Mis

mation can be obtained from: www.sscs.org/chapter/awardnews.htm.

Sister Society Agreement with VDE/ITG

The AdCom agreed to enter into a Sister Society Agreement with VDE/ITG. VDE is the German National EE Association, and ITG is its Information Technology Society. The SSCS VDE/ITG Sister Society Agreement consists of a mutual exchange of privileges on:

- conference paper submissions
- conference registration at member rates
- appropriate form of cosponsorship of conferences
- same admission fee (if any) for Distinguished Lecture events

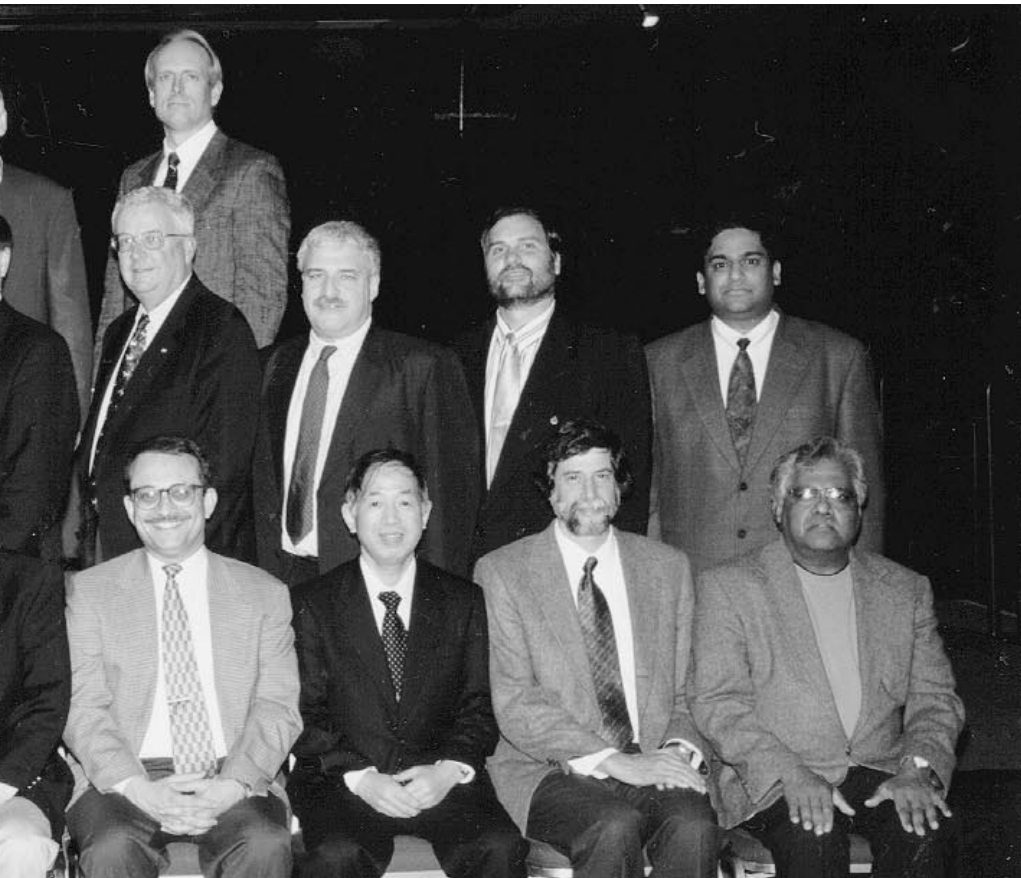
The Sister Society Agreement with VDE/ITG was initiated by the IEEE Germany Section and the IEEE Communications Society. An um-

brella agreement between IEEE and VDE was already in place. The IEEE Communications, Circuits and Systems, and Information Theory Societies have already signed the Sister Society Agreement with VDE/ITG.

ISSCC Digital Archive

Preparation and production of a digital archive of ISSCC digests from 1955 to 2002 was authorized by the AdCom on 28 August 1999. At the February 2000 AdCom meeting, additional components were authorized to enhance the utility of the ISSCC CD album. This includes hyperlinked citations and references and the cost of conversion of the ISSCC Slide Supplements. The ISSCC Digital Archive is expected to be available for purchase at the 2001 ISSCC.

Improvements were also planned and funded for the JSSC subject



r Svensson, Bob Swartz, Bruce Wooley (President), Asad Abidi (Secretary), Toshiaki Masuhara, Rudy van de Plassche, Steve Kosonocky, Neil Weste, Dave Hodges (Treasurer), Eby Friedman, Ser-
sing: Lew Terman (Past President), Jan Van der Spiegel

- TSA-VLSI 2001
- Asia-Pacific ASIC for both 2000 and 2002 and to fund the 2000 AP-ASIC with a \$10,000 grant

Budget

The AdCom has fiduciary responsibility for an annual budget of over \$2 million with assets of over \$3 million. Treasurer Dave Hodges reported on the financial health of the Society and presented a balanced preliminary budget for 2001. The page budget for the *JSSC* for 2001 was approved at 2,100 pages. The *Journal* published 2,068 pages in 1999 and 2,352 pages in 1998. The financial health of the Society continues to be excellent.

Call for Increased Services to Society Members

The AdCom ended its meeting with a challenge to suggest better ways of serving members in line with the core purpose and technical expertise of the Society and to take advantage of its financial health. John Corcoran agreed to collect suggestions in order to present topics for further discussion at the August AdCom. Members are welcome to propose suggestions for Society programs by emailing John at john_corcoran@agilent.com. ●

index, including hyperlinking of the references. The result will be an improved merged *JSSC/ISSCC Digest* master index. The budget for the two projects is now \$235K.

www.sscs.org/meetings/. At the February 2000 meeting, the Society agreed to technically cosponsor:

ISSCC 2001 Short Course on CD

Continuing the successful introduction of a CD of the ISSCC Short Course for 2000, the AdCom has agreed to fund another Short Course for 2001. The CD version of the 2001 Short Course is planned to utilize the Online Video-on-Demand already available through IEEE at <http://ieeemediaplatform.com/vod/iee/>.

Meetings Supported

The SSCS technically cosponsors a select list of meetings each year. These meetings are always listed in the Events Calendar at the back of this newsletter and online at

Solid-State Circuits Society Newsletter



The Publications Committee recommendations that the AdCom approved include: funding the Digital Archives of the ISSCC 1955–2002, improvements of indexing for both the ISSCC and JSSC electronic collections, and a page budget for the *Journal of Solid State Circuits* in 2001.

The members of the Publications committee are I-r: Steve Lewis (JSSC Editor), Dave Hodges, Dick Jaeger (Chair), Asad Abidi, Rudy van de Plassche, Tim Tredwell.

SSCS Members Honored as 2000 IEEE Fellows

Welcome and congratulations to the following new IEEE Fellows! The IEEE Board of Directors has recognized these professionals for their outstanding and extraordinary qualifications and experience. Each award is distinguished by the particular contributions made by the recipient.

No more than one-tenth of 1% of the total Institute membership may be advanced to Fellow grade in any given year. Of the 248 Senior members advanced in 2000, 23 were members of the Solid-State Circuits Society. The seven introduced in the April issue of the Newsletter were evaluated by the SSCS, rated and ranked by the 26-member IEEE Fellows Committee, and received their Fellow Certificates at the ISSCC

last February. The other 16 have also been rated and ranked by the 26-member IEEE Fellows Committee but initiated their nomination process through another of IEEE's many technically related Societies. The contributions of all these professionals has helped to mold and advance our field to the outstanding industry that the world recognizes today.

Forms for nominating and recommending Fellows are typically available in late November for an application deadline of the following 15 March. Members may apply for Senior membership, which is a precondition of the Fellow distinction, at any time during the year. URL: www.ieee.org/organizations/rab/md/smforms.htm.

Peter M. Asbeck

For development of heterostructure bipolar transistors and applications.

Peter Asbeck received the B.S. and Ph.D. degrees from the Electrical Engineering Department, Massachusetts Institute of Technology, Cambridge, in 1969 and 1975, respectively. He was with the Sarnoff Research Center, Princeton, NJ, and Philips Laboratory, Briarcliff Manor, NY, working in the areas of quantum electronics and GaAlAs/GaAs laser physics and applications. In 1978, he joined Rockwell International Science Center, where he was involved in the development of high-speed devices and circuits based on III-V compounds and heterojunctions. He pioneered the effort to develop heterojunction bipolar transistors based on GaAlAs/GaAs and InAlAs/InGaAs materials and has contributed widely to the areas of physics, fabrication, and applications of these devices.

In 1991, Dr. Asbeck joined the University of California, San Diego, as Professor in the Department of Electrical and Computer Engineering. His research interests are in the development of high-speed

heterojunction transistors and optoelectronic devices and their circuit applications.

Dr. Asbeck's research has led to more than 190 publications, 10 book chapters, and 10 patents. He was the General Chairman of the 1996 Device Research Conference. He received the Leonardo Da Vinci award from Rockwell in 1986, and is a Distinguished Lecturer of the IEEE Electron Devices Society.

Werner Bächtold

For contributions to the development of microwave semiconductor devices and circuits.

Werner Bächtold received the diploma and the Ph.D. degree in electrical engineering from the Swiss Federal Institute of Technology, Zurich, in 1964 and 1968, respectively. From 1969 to 1987, he was with the IBM Zurich Research Laboratory. He has contributed to the development of the Gallium-Arsenide MESFET technology; in particular, he investigated the microwave noise properties and demonstrated the first X and Ku-band MESFET amplifiers.

In the area of superconducting devices and circuits, Dr. Bächtold designed logic and memory cir-

cuits with Josephson junctions. He demonstrated the first non-latching Josephson logic circuit. In a project on semiconductor lasers for digital communication, Dr. Bächtold contributed to laser modeling and design. He had several assignments at the IBM T. J. Watson Research Center, Yorktown Heights, NY.

Since December 1987, Dr. Bächtold has served as Professor of Electrical Engineering at the Swiss Federal Institute of Technology, Zurich. He is leading the Microwave Electronics Group at the Laboratory for Electromagnetic Fields and Microwave Electronics and teaches on the subjects of microwave techniques and electronics. The research activities of his group are focused on: (1) the design and characterization of monolithic microwave integrated circuits (MMICs) based on various technologies, (2) microwave measurement techniques, (3) technology and design of Indium Phosphide HEMT (high electron mobility transistors) devices and millimeter-wave integrated circuits, and (4) microwave-optoelectronics.

Karl Wayne Current

For contributions to the development and design of multiple valued logic circuits and education in electronic circuits.



Karl Wayne Current received the Ph.D. degree in electrical engineering from the University of Florida, Gainesville, in 1974. He worked as a designer of LSI ECL at TRW Systems Group in Redondo Beach, CA. In 1976, he joined the faculty of the Electrical Engineering Department of the University of California, Davis, where he is now Professor. Since 1977, he has been a licensed Consulting Professional Electrical Engineer in California, serving as a consultant to the electronics industry, a government laboratory, and various government agencies.

Dr. Current is interested in analog and digital electronic circuits, integrated circuit design, multiple valued logic, and computer aided circuit design. He has served as the General Chair of the 1993 IEEE Computer Society International Symposium on Multiple Valued Logic, Chair of the IEEE Computer Society Technical Committee on Multiple Valued Logic in 1991 and 1992, Technical Program Chair for the 1983 and 1991 IEEE Computer Society International Symposia on Multiple Valued Logic, Chair of the Sacramento Section of the IEEE Circuits and Systems and Automatic Control Groups in 1979 and 1980, Local Arrangements Chair of the IEEE Midwest Symposium on Circuits and Systems in 1997, Member of the Technical Program Committee of the IEEE Southwest Symposium on Mixed Signal Design in 1999 and 2000, and is an Associate Editor of *Multiple Valued Logic: An International Journal*. Dr. Current is also a member of Eta Kappa Nu, Tau Beta Pi, Sigma Xi, and Phi Eta Sigma honorary societies.

Michel J. Declercq

For contributions to the development and design of multiple valued logic circuits and education in electronic circuits.

Michel J. Declercq received the Electrical Engineering and Ph.D. degrees from the Catholic University of Louvain, Belgium, in 1967 and 1971, respectively. In 1973, he was awarded a Senior Fulbright Fellowship



and joined Stanford University, Stanford, CA as a Research Associate in the Microelectronics Labs. From 1974 to 1978, he was Research Associate and lecturer at the Catholic University of Louvain, Belgium. In 1978, he joined Tractebel in Brussels, Belgium, where he was Group Leader of the Electronic Systems team.

In 1985, Dr. Declercq joined the Swiss Federal Institute of Technology (EPFL), Lausanne, where he is currently Professor and Director of the Electronics Laboratory. From 1993 to 1995, he served as Chairman of the Electrical Engineering Department. His research activities are related to mixed analog-digital IC design and design methodologies. He is more particularly involved in low-power/low-voltage circuits, high-frequency circuits for telecommunications, fully depleted SOI technology and circuits, and high-voltage circuits for MEMS applications and others. He is author and coauthor of more than 150 scientific publications and two books and holds several patents. Dr. Declercq serves as an expert with the European Commission for scientific research programs in information technologies.

Eby Gershon Friedman

For contributions to high-performance circuit design and VLSI-based synchronous systems.

Eby G. Friedman received the B.S. degree from Lafayette College, Easton, PA, in 1979, and the M.S. and Ph.D. degrees in electrical engineering from the



University of California at Irvine in 1981 and 1989, respectively.

From 1979 to 1991, Dr. Friedman was with Hughes Aircraft Company, rising to the position of manager of the Signal Processing Design and Test Department, responsible for the design and test of high-performance digital and analog ICs. He has been with the Department of Electrical and Computer Engineering at the University of Rochester, Rochester, NY, since 1991, where he is a Professor and Director of the high-performance VLSI/IC Design and Analysis Laboratory and the Director of the Center for Electronic Imaging Systems. His current research and teaching interests are in high-performance synchronous digital and mixed-signal microelectronic design and analysis with application to high-speed portable processors and low-power wireless communications.

Dr. Friedman is the author of approximately 150 papers and book chapters and is the author or editor of four books in the fields of high-speed and low-power CMOS design techniques, interconnect and substrate noise, pipelining and retiming, and the theory and application of synchronous clock distribution networks. He is a Regional Editor of the *Journal of Circuits, Systems, and Computers*, a member of the editorial board of *Analog Integrated Circuits and Signal Processing* and the *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Chair of the Steering Committee for the *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, a Distinguished Lecturer of the IEEE CAS Society; a member of the IEEE Circuits and Systems (CAS) Society Board of Governors; CAS liaison to the IEEE Solid-State Circuits Society; a member of the technical program committee for a number of conferences; and a Fulbright Scholar.

Continued on next page →

Manfred Glesner

For contributions to the development of microelectronic system design and education in microelectronics.

Professor Dr. h. c. Manfred



Glesner was born in Saarlouis, Germany in 1943. He received the diploma in Applied Physics and Electrical Engineering from Saarland University, Saarbrücken, Germany, in 1969. In 1975, he received the Ph.D. degree from the same university for his research on tolerance optimization techniques in computer aided circuit design.

In 1981, Dr. Glesner became Associate Professor at Darmstadt University of Technology, Darmstadt, Germany, where, since 1989, he has been the head of the Institute for Microelectronic Systems. In 1982, he was the first to run a multiproject chip at a German university as a regular course offering. Currently he is director of a Graduate School for Intelligent Systems in Information Technology. He teaches courses in microelectronic circuit design and CAD for microelectronics.

Dr. Glesner has contributed original research in the topics of high-level synthesis and physical design, especially for deep submicron technologies. Moreover, he is responsible for a special research program (Sonderforschungsbereich) of the German National Science Foundation (DFG) for microelectronic system design in mechatronics. He has successfully organized several national and international microelectronic conferences, and he organized and participated in many national and international large-scale research projects. Dr. Glesner has been a project consultant for the European Commission and United Nations Industrial Development Organization. After the political breakdown in

Eastern Europe, he built up several microelectronics design centers at universities with support from the European Union based TEMPUS-Program. For his contributions to the field of microelectronics, he has received two honorary causa doctoral degrees as well as one honorary causa professorship.

Daniel Charles Guterman

For leadership in the development of non-volatile, solid-state memory technologies.

Dr. Daniel C. Guterman received the B.S.E.E. degree (summa cum laude) from Tufts University, Medford, MA, in 1970, and the M.A. and Ph.D. degrees from Princeton University, Princeton, NJ, in 1972 and 1976, respectively.

Dr. Guterman is a Fellow of SanDisk Corporation, having joined the company in 1989 as Director of Advanced Technology, leading its pioneering effort in developing SanDisk's revolutionary D2 FLASH multilevel storage "logical scaling" technology. Previously, he was involved in and managed development programs that span a wide range of non-volatile memory technologies, including EPROMs and EAROMs at Texas Instruments and Mostek, followed by NOVRAMs and EPROMs at Xicor, where he invented its workhorse "direct write" EEPROM cell. He is named as inventor in over 30 patents and has coauthored more than 10 technical articles.

Lawrence Ernest Larson

For contributions to development and applications of high-speed integrated circuits and devices.

Lawrence E. Larson received the B.S. degree in electrical engineering in 1979 and the Masters in Engineering degree in 1980, both from Cornell University, Ithaca, NY. He received the Ph.D.



degree in electrical engineering from the UCLA in 1986.

Dr. Larson has been involved in the development of ultrahigh frequency compound semiconductor transistor and integrated circuit technology. During the late 1980s he was a key member and leader of the team at Hughes Research Laboratories that developed the first high-reliability InP-based HEMT technology for spaceborne 60-GHz low-noise amplifier applications. These millimeter-wave amplifiers provided a dramatic improvement over prior generations of mmW low-noise amplifiers, dropping receiver noise figure from 12 dB to less than 2.5 dB. In addition, he led the research group that extended InP-based HEMT technology into the integrated circuit area. His group was the first to demonstrate a high-performance InP-based MMIC technology. His research led to a number of "firsts," including the first 44-GHz InP-based HEMT MMIC power amplifiers, with greater than 40% power-added efficiency; a 2-GHz low-noise MMIC amplifier with a noise figure of under 0.5 dB; and the world's fastest room-temperature millimeter-wave integrated circuit: a VCO operating in the fundamental mode in excess of 210 GHz.

Dr. Larson led the research effort in the early 1990s that developed the first microwave and millimeter-wave applications of microelectronic-mechanical (MEMS) technologies, including the first MEMS switches for microwave applications. Dr. Larson holds many of the fundamental patents in this field. He also led the technical effort with a Hughes/IBM alliance for developing commercial applications of Si/SiGe HBT technology. His group was the first to use this technology to demonstrate high-performance, microwave/millimeter-wave (1025 GHz) ICs in silicon-based technology in the early 1990s.

Dr. Larson joined the faculty of the University of California-San Diego in 1996, where he is the inaugural holder of the Communications Industry Chair. He is currently Co-Director of the UCSD Center for Wireless Communications. He was corecipient of the 1996 Lawrence A. Hyland Patent Award of Hughes Electronics for his work on low-noise millimeter-wave HEMTs and the 1999 IBM Microelectronics Excellence Award for his work in Si/SiGe HBT technology. He has published over 120 papers, coauthored and edited two books and holds 21 U.S. patents.

Yong Ching Lim

For contributions to the design of FIR digital filters.

Yong Ching Lim received the A.C.G.I. and B.Sc. degrees in 1977 and the D.I.C. and Ph.D. degrees in 1980, all in electrical engineering, from Imperial College, University of London, U.K.



From 1980 to 1982, he was a National Research Council Research Associate at the Naval Postgraduate School, Monterey, CA. Since 1982, he has been with the Department of Electrical Engineering, National University of Singapore, where he is currently a Professor. His research interests include digital signal processing and VLSI circuits and systems design.

Dr. Lim was selected to receive the 1996 IEEE Circuits and Systems Society's Guillemain-Cauer Award, the 1990 IREE (Australia) Norman Hayes Award, the 1977 IEE (U.K.) Prize, and the 1974-77 Siemens Memorial (Imperial College) Award. He served as an Associate Editor for the *IEEE Transactions on Circuits and Systems* from 1991 to 1993 and again since 1999. He has also served as an Associate Editor for *Circuits, Systems and Signal Pro-*

cessing from 1993 to 2000. He is the current Chairman of the DSP Technical Committee of the IEEE Circuits and Systems Society. He served in the Technical Program Committee's DSP Track as the Chairman in ISCAS'97 and ISCAS'00 and as a Cochairman in ISCAS'99.

Jaime Ramírez-Angulo

For contributions to design methodologies for analog signal processing integrated circuits.

Jaime Ramírez-Angulo received the B.S.E.E. and M.S.E.E. degrees from the National Polytechnic Institute, Mexico City, Mexico, and the Ph.D. degree in engineering from the University of Stuttgart, Stuttgart, Germany, in 1974, 1976, and 1982, respectively.

Dr. Ramírez-Angulo is Professor and Director of the VLSI laboratory at the Klipsch School of Electrical and Computer Engineering, New Mexico State University (NMSU), Las Cruces. He also serves as Director of the NASA Center for Autonomous Control Engineering at NMSU. His research is related to VLSI circuit design: mixed-mode test techniques, low-voltage, BiCMOS, neuro-fuzzy analog circuits and special purpose analog coprocessors, Wideband Amplifier Design, High Frequency Filters and Current-Mode signal processing. He was the Technical Chairman of the 26th Midwest Symposium on Circuits and Systems in Puebla, Mexico, in 1983, and the General Chairman of the 42nd Midwest Symposium on Circuits and Systems in Las Cruces, NM, in August 1999. From 1982 to 1984, he was a researcher at the National Institute for Astrophysics Optics and Electronics (INAOE) in Mexico. From 1984 to 1990, he was Assistant Professor at Texas A&M University, College Station.



Dr. Ramírez-Angulo is a member of the Analog Signal Processing Committee of the IEEE CAS Society and a member of the Steering Committee of the Midwest Symposium on Circuits and Systems. He has published 176 technical papers and has received funding from prestigious sources such as NSF, Sandia National Labs, NASA/ACE, Texas Instruments, and the AFOSR. He has held numerous invited and plenary presentations.

Ronald D. Schrimpf

For contributions to the understanding and the modeling of physical mechanisms governing the response of semiconductor devices to radiation exposure.

Ronald D. Schrimpf received the B.E.E., M.S.E.E., and Ph.D. degrees from the University of Minnesota, Minneapolis, in 1981, 1984, and 1986, respectively. His graduate work dealt with three-dimensional integrated circuits. He joined the University of Arizona, Tucson, in 1986, where he served as Assistant Professor, Associate Professor, and Professor of Electrical and Computer Engineering. He has been a Professor of Electrical Engineering at Vanderbilt University, Nashville, TN, since 1996.



Dr. Schrimpf's research focuses on radiation effects and reliability in semiconductor devices, including low-dose-rate effects in CMOS and bipolar integrated circuits, single-event effects in linear integrated circuits and power devices, and development of Technology Computer Aided Design (TCAD) tools for radiation effects. He has authored or coauthored more than 140 publications in the areas of semiconductor devices, radiation effects, and reliability.

Dr. Schrimpf served as General Chairman of the 1999 IEEE Nuclear

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and Space Radiation Effects Conference (NSREC) and previously served the NSREC as Technical Program Chairperson, Guest Editor, and Session Chairperson. He is a three-time recipient of the Outstanding Paper Award at the NSREC and was awarded the 1996 IEEE Nuclear and Plasma Sciences Society Early Achievement Award. In addition, he has served on the Technical Program Committees of the IEEE International Devices Meeting (IEDM) and the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM). He is currently the Principal Investigator of a Multi-Disciplinary University Research Initiative (MURI) in the area of Semiconductor Radiation Physics.

Mani Soma

For contributions to mixed analog-digital system design-for-test.

Mani Soma received the B.S.E.E.



degree from California State University, Fresno, in 1975, and the M.S. and Ph.D. degrees from Stanford University, Stanford, CA, in 1977 and 1980, respectively.

From 1980 to 1982, Dr. Soma was with the General Electric Research and Development Center (Schenectady, NY), working on design and test methodologies for VLSI integrated circuits and systems. He then joined the Department of Electrical Engineering at the University of Washington, Seattle, and has been a Professor since 1988. He was the Associate Director of the NSF Center for Design of Analog-Digital ICs from 1989 to 1994.

Dr. Soma founded and chaired the IEEE Mixed-Signal Test Bus Standard Working Group (1149.4) from 1991 to 1995 and remains active in standard development. He was Technical Program Chair for ISCAS 1995 and helped originate the Pacific Northwest Test Work-

shop, which has become the annual IEEE International Mixed-Signal Testing Workshop. He received the IEEE Computer Society Meritorious Service Award (1995) and the IEEE Computer Society Golden Core Award (1997). He has published papers in electronic design, test, and reliability; and has more recently focused on research in mixed analog-digital system design and test.

Costas J. Spanos

For contributions and leadership in semiconductor manufacturing.

Costas J. Spanos received the Electrical Engineering Diploma from the NTUIA, Greece, in 1980, and the M.S. and Ph.D. degrees in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, in 1981 and 1985, respectively.



From 1985 to 1988, Dr. Spanos was with Digital Equipment Corporation. He joined the University of California at Berkeley in 1988, where he is now a Professor of Electrical Engineering and the Director of the Berkeley Microfabrication Laboratory. His current work focuses on Novel sensor, flexible manufacturing systems, and statistical design techniques for ICs.

Dr. Jack Y. C. Sun

For contributions to advanced CMOS technology.

Jack Y. C. Sun received the Ph.D. degree from the University of Illinois, Urbana, in 1983.

Dr. Sun is presently Director of Logic Technology Division at TSMC. Until mid-1997, he was senior-level manager at the IBM T. J. Watson Research Center, Yorktown Heights, NY, and SRDC. From 1988 to 1992, he managed the bipolar technology group, which set a number of records in Si BJT npn and pnp devices, including, in

1989–1990, the demonstration of a 75-GHz SiGe HBT and sub-25-ps Si and SiGe ECL circuits. He is cited for contributions to advanced CMOS technology and was the first to develop dual-poly (n+/p+) 0.5- μm room- and low-temperature CMOS technology and to overcome boron penetration problems. He played a key role in the identification and understanding of polysilicon depletion and boron penetration effects in <0.25- μm thin-oxide CMOS technologies. Together with Drs. C. T. Sah and J. Tzou, in 1981–1983, he was the first to identify the hydrogenation of boron acceptors during hot carrier injection in MOS structures. In the area of SOI, in 1995–1996 he led the work in clarifying the floating-body effects in SOI devices and circuits and the development of a pulse-IV technique to overcome heating problems. He has authored or coauthored over 200 papers and many invited papers on CMOS, SiGe bipolar, BiCMOS, and SOI. He also holds a key patent on SOI transistor structure with high-mobility SiGe channels, and seven U.S. patents. He is a coinventor of a self-aligned SiGe HBT structure. He was also the key integration architect/driver of high-performance self-aligned SiGe ECL-CMOS and BiCMOS processes at IBM.

Federico Tosco

For contributions and leadership in technologies and international standards for optical and wireless communications.

Federico Tosco received the



Doctorate of Engineering degree from the Polytechnic of Turin, Italy, in 1964.

In 1965, he joined CSELT, the R&D laboratories of the Telecom Italia Group (then SIP), where he held various positions. Since 1991, he has been responsible for the Mobile

Services division. Previously he spent many years managing several R&D projects in the optical communications field, including the project that led to the first installation of an optical cable in the Italian telecommunication network. He is author or coauthor of some 60 papers, including several invited papers.

Since 1968, Dr. Tosco has been active in international standardization, holding various important positions. In particular, from 1989 to 1996 he was Chairman of the Optical Communications Working Party of the ITU-T Study Group 15 (Transmission Systems and Equipment). He is now Vice-Chairman of ITU-T Study-Group 16 (Multimedia

Services and Systems) and Chairman of the working party in charge for multimedia communication, in particular over the Internet. He is active in the IEEE Communications Society, where he is Vice-President of Society Relations. Recently, he was Cochair of the MMT'99 (Multi-Access Mobility and Teletraffic for Wireless Communications) workshop and was a main organizer of the ICUPC'98 (International Conference on Wireless Personal Communications) conference.

Bogdan Maciej Wilamowski

For contributions to industrial electronics and static induction devices.

Bogdan M. Wilamowski received the M.S. degree in computer engineering and the Ph.D. degrees in neural computing and integrated circuit design in 1966, 1970, and 1977, respectively, from the Technical University of Gdansk, Poland.

He received the title of Professor from the President of Poland in 1987. He was the Director of the Institute of Electronics (1979–1981) and the Chair of the Solid State Electronics Department (1987–1989) at the Technical University. Since 1989, he has been with the University of Wyoming, Laramie. From 1968–1970, he was with the Nishizawa Laboratory at Tohoku University, Japan, and spent one year at the Semiconductor Research Institute, Sendai, Japan as a JSPS Fellow (1975-1976). He was a Visiting Scholar at Auburn University, Auburn, AL (1981-1982 and 1995-1996), and a Visiting Professor at the University of Arizona, Tucson (1982-1984). He is the author of four textbooks, more than 200 refereed publications, and 27 patents. His main areas of interest are digital hardware, electronics, CAD development, VLSI, network programming, and neuro-fuzzy systems.

Dr. Wilamowski has been, and currently is, a member of organizing/technical committees of several IEEE International Conferences: ICIPS'98 (Australia), ISIE'98 (South Africa), ISIE'99 (Slovenia), IECON'99 (U.S.), ICRAM'99 (Turkey), ICIT'00 (India), IECON'00 (Japan), IIZUKA'00 (Japan), ICMNFBS'00 (France), ISIE'01 (Korea), and IECON'02 (Spain). He serves also as the General Chair of IECON2001 in Denver, CO. He is the treasurer of the IEEE Industrial Electronics Society and a member of the IEEE Neural Network Council. He is Associate Editor of the *IEEE Transactions on Neural Networks*, the *IEEE Transactions on Education*, and the *IEEE Industrial Electronics Newsletter*. ●



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Lewis M. Terman
IBM Research
Yorktown Heights, NY

Elected AdCom to 12/31/00:

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Sergio Bampi
David Hodges
Toshiaki Masuhara
Rudy van de Plassche

Elected AdCom to 12/31/01:

Gerhard Fettweis
Mark Horowitz
Richard C. Jaeger
Charles G. Sodini
Neil Weste

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Anantha Chandrakasan
John Corcoran
Chris Mangelsdorf
Willy Sansen
Christer Svensson

Other Representatives:

Representative from CAS to SSCS
Eby G. Friedman
Representative to CAS from SSCS
T. R. Viswanathan

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Chapters	Jan Van der Spiegel
Educational Activities	Kevin O'Connor
Meetings	Mark Horowitz
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Nominations	Robert G. Swartz
Publications	Richard C. Jaeger

Solid-State Circuits Technology

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For detailed contact information, see the Society Web page: www.sscs.org/info/

For questions regarding Society business, contact the SSCS Executive Office.

Contributions for the Oct. issue of the newsletter must be received by 1 Aug. at the SSCS Executive Office.

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Independent Short Courses

KeeP these upcoming courses in mind. The dates and exact locations are still being determined. These one-day courses are tailored to experienced engineers who are looking for a short burst of intense information on the latest technologies to keep them abreast of current developments in various cutting-edge subjects related to devices and circuits. Priced between \$500 and \$700, these courses may also be priced differently for later online delivery in their recorded form. For more information on these new short courses please visit www.ieee.org/organizations/society/eds/2000courses.html.

Circuit Designs and Technology for RF-CMOS

By Asad Abidi (UCLA)

Location: Austin, TX

Date: Last week of July

Dr. Abidi will focus on; low noise amplifiers, mixer circuits, oscillator circuits, and on-chip passive components. An acknowledged expert on integrated circuits for wireless communications, Dr. Abidi is one of the three editors of a just published IEEE book on wireless communications entitled "Integrated Circuits for Wireless Communications."

Device, Circuit, and Reliability Modeling for the Silicon Industry

By Dr. Sanjay Banerjee, University of Texas (UT) at Austin

Location: Austin, TX

Date: Fall 2000

Devices and Circuits for Fiber Optical Communications

By Dr. Joe Campbell, UT

Location: San Francisco Bay Area

Date: Fall 2000 ●

What's New @ IEEE in Circuits

"What's New @ IEEE" is an opt-in email newsletter service that provides monthly updates on IEEE activities, technology trends, career development tips, member benefits, upcoming conferences, and new products. "What's New @ IEEE in Circuits" is one of eight new complimentary electronic newsletters. Select the email update services in the field that is right for you: Circuits, Communications, Computing, Signal Processing, Wireless, Members, and Graduates of the Last Decade. Members and customers can subscribe to one or more of these at www.ieee.org/whats-new.

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Events Calendar *continued from page 20*

Also posted on www.sscs.org/meetings

Technically Co-sponsored Meetings

MTDT 2000

IEEE International Workshop on Memory Technology, Design and Testing

7–8 August 2000

Fairmont Hotel, San Jose, CA

Contact: Rochit Rajsuman

Tel: +1 408 727 2222 ext. 386

Email: r.rajsuman@advantest.com

AP-ASIC

Asia-Pacific Conference on ASICs

www.ap-asic.org

28–30 August 2000

Cheju, Korea

Deadline for submission of camera-ready pdf papers: passed

Contact: AP-ASIC'00

Research Institute of ASIC Design

Yonsei University, Seoul, Korea

Tel: +82 2 361 3523

Fax: +82 2 364 8162

Email: asic2000@ap-asic.org

ESSCIRC 2000

European Solid-State Circuits Conference

www.eescirc.org

19–21 September 2000

Kista Technology Park, Stockholm, Sweden

Paper deadline: passed

Contact: Hannu Tenhunen

Royal Institute of Technology

Kista, Sweden

Tel: +46 8 752 1142, +46 70 733 5748

Fax: +46 8 752 1140

Email: hannu@ele.kth.se

BCTM: IEEE Bipolar/BiCMOS Circuits and Technology Meeting

ectm.et.tudelft.nl/www/BCTM/

24–26 September 2000

Minneapolis Marriott City Center

Minneapolis, MN

Contact: Janice Jopke

CCS Associates

Eden Prairie, MN

Tel: +1 612 934 5082

Fax: +1 612 934 6741

Email: jopke@aol.com

GAASIC

Gallium Arsenide Integrated Circuits Symposium

www.gaasic.org

5–8 November 2000

Westin Hotel, Seattle, WA

Paper Deadline: passed

Contact: James J. Komiak

Sanders, A Lockheed Martin Co.

Nashua, NH

Email: james.j.komiak@lmco.com

2001 VLSI-TSA

International Symposium on VLSI Technology, Systems, and Applications

www.erso.itri.org.tw/VLSI-TSA/

18–20 April 2001

Taipei, Taiwan, R.O.C.

Paper Deadline: October 20, 2000

Contact: Ran-Hong Yan

Lucent Technologies

Holmdel, NJ

Tel: +1 732 949 7695

Email: rhy@lucent.com

SSCS EVENTS CALENDAR

Also posted on www.sscs.org/meetings

2001 ISSCC

International Solid-State Circuits Conference

www.isscc.org

5-7 February 2001

San Francisco Marriott Hotel, San Francisco, CA

Paper submission deadline: 6 September 2000

(See new electronic submission requirements on the Web site)

Contact: Courtesy Associates
Washington, DC

Tel: +1 202 331 2000

Fax: +1 202 331 0111

Email: ISSCC@courtesyassoc.com

2000 Biomedical Electronics SSCTC Workshop

www.sscs.org/ssctw/oct00.htm

12-13 October 2000

Key Bridge Marriott, Arlington, VA

Contact: Suzanne Demarie
Courtesy Associates
Washington, DC

Tel: +1 202 331 2000

Fax: +1 202 973 8722

Email: SSCTC@courtesyassoc.com

2001 CICC Custom Integrated Circuit Conference

www.his.com/~cicc/

6-9 May 2001

San Diego, CA

Paper deadline: 29 November 2000

Contact: Ms. Melissa Widerkehr
Widerkehr & Associates
Gaithersburg, MD

Tel: +1 301 527 0902

Fax: +1 301 527 0994

Email: cicc@his.com

2001 Symposium on VLSI Circuits

www.bcasj.or.jp/vlsi_sym/

14-16 June 2001

Rihga Royal Hotel, Kyoto, Japan

Deadline for receipt of summaries: 10 January 2001

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Continued on page 19

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