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# SOLID-STATE CIRCUITS

IEEE Solid-State Circuits Society Quarterly Newsletter



## New DVD Includes All JSSC and ISSCC Papers: the Solid-State Circuits Digital Archive 2000 DVD

This August, the Society will be issuing the Solid-State Circuits Digital Archive 2000. This complete archive comes on a single DVD and contains not only the complete archive through 2000 of all the issues of the Journal of Solid-State Circuits (JSSC) from 2000 back to the first issue in 1966, but also includes the Digests of the International Solid-State Circuits Conference (ISSCC), starting with 1955.

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Presented through a user-friendly browser portal, articles can be located by date, author, or a single-subject index expanded from the year-end printed indexes of the JSSC. Tables of contents of issues have the same familiar look as the published *Journal* tables of contents or the conferences' Sessions listing. Each article's abstract summary screen provides:

- a formatted text citation ready to paste into a user's article in composition
- links to the authors' bios
- links effective on the disk to references the authors cited
- links effective on the disk forward to more-recent articles that have cited the work
- the list of subjects identified in the index
- for ISSCC articles, a link to the presentation slides in the slide supplement.

"This version is easier to use than our previous CD and DVD issues of

the Society," according to Richard C. Jaeger, chair of the Publications Committee who reviewed the prototype. "It's cool. I like the format; it uses lots of hyperlinks that make browsing more effective."

After searching from a list of keywords, an article's abstract shows all the related keywords for that selection. You can search directly from that list of keywords, or you can choose to view the list of all the works of one of the coauthors, or return directly to the table of contents for that issue. The back button allows more intuitive navigating.

The pages of the articles are available in Adobe Portable Document Format (.pdf) for printing and text searching. Additionally, Acrobat allows the sorting of search results by date. Board and committee listings, awards, letters to the editors, and calls for papers are other ephemera included to make this archive complete.

*Continued on next page*

## Solid-State Circuits Digital Archive 2000


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The AdCom thanked Tim Tredwell (right) for his outstanding leadership and contributions to the development and success of the Electronic Archives of the Society. Society President Bruce Wooley presented a plaque to Tredwell in recognition. This year, Tredwell begins serving as the Chairman of the Executive Committee of the International Solid-State Circuits Conference.

### How to Order

Because the DVD was included as part of the registration fee, registrants at the 2001 ISSCC will automatically receive the new DVD in the mail. Others can order through the IEEE.



SSCS Publications Committee, February 2001. (l-r) Tim Tredwell, Lew Terman, Richard Jaeger, Asad Abidi, and David Hodges. The SSCS AdCom approved two recommendations of the Publications Committee: (1) to include all issues of the *Digests of the Symposium on VLSI Circuits* in a new Digital Archive DVD to be available spring 2002. The DVD will be an archive for all papers from the *JSSC*, *ISSCC*, and *VLSI Circuits* and (2) to send a special issue of the *IEEE Transactions on Microwave Theory and Techniques on Integrated and Nonintegrated Silicon RF and Microwave Circuits* to all SSCS members in winter 2001.

### The Annual CD

The annual update CD-ROM of the *JSSC* for the years 1999-2000 is being issued and mailed to all SSCS members in August. This annual update to the complete *JSSC* on CD Collection also contains the Master Index to all previous issues so one can search on titles, keywords, and authors and

review all the article abstracts. This year, the Master Index will also include search data for all the papers and sessions of the ISSCC. A complete set of the *JSSC* articles from the first issue in 1966 is available on CD. Search for *JSSC* at [www.shop.ieee.org/store](http://www.shop.ieee.org/store). The ISSCC papers are only available on DVD. ●

## Improved IEEE *Xplore*<sup>™</sup>

### Better Stability and Accessibility

Behind your screen of IEEE *Xplore*<sup>™</sup> in recent months, the IEEE has upgraded hardware and authentication database software, streamlined communications pipelines, and better controlled intelligent agents that occasionally choke the system. During the problem episodes last November when system availability was inconsistent, the IEEE chose to allow users to pass through unauthenticated. Member users might have experienced such times as good luck, permitting access to publications to which they didn't subscribe, including a wealth of conference proceedings. Other times the traffic overload caused users to experience extremely slow site performance. By early March 2001, with the continuing behind-the-scenes improvements and testing, users experienced fewer glitches, smoother log-ons, and quick-

er response times. "Based on conversations with librarians who subscribe to online subscriptions through IEEE *Xplore*<sup>™</sup>, customer satisfaction has improved and complaints are down," according to Barbara Lange, senior product manager, IEEE Publishing Business Development.

### Renewal Options

When renewing subscriptions and membership this fall, members will be confronted with a wide variety of options to optimize their online access across all the Societies' offerings. The SSCS offers the *JSSC* monthly print subscription, online access, and 2 years of CD archival access bundled for one fee. Other Societies offer separate pricing for online access. Some Societies offer one print subscription price combined with multiple-subscription online access. The IEEE is working

to normalize access rules across Societies, but it may take a few years to settle on the preferred formula.

### Expect Quality

With a continuous process of improvement, users' comments are important. If your search returns obvious mismatches or omissions, please take a few minutes to notify the IEEE. Although we can't correct original errors in the printed copy, we can make sure that search criteria work as effectively as possible. Email the details to [iel-trace@ieee.org](mailto:iel-trace@ieee.org). If your comments apply to SSCS-issued publications, either our conferences or the *JSSC*, also copy your email to [sscs@ieee.org](mailto:sscs@ieee.org). Corrections made to the online versions may also be required on the digital masters of the Solid-State Circuits Digital Archive so that future issues of the DVD and CD products remain up to date. ●

# Low Power Electronics and Design Symposium Preview

This year, the International Symposium on Low Power Electronics and Design is scheduled for 6–7 August 2001 at the Hilton Waterfront Beach Resort in Huntington Beach, CA, with 12 presentation sessions and four poster sessions on the agenda. The Symposium will open with the keynote speech: “Wireless beyond the third generation: Facing the energy challenge,” by Jan Rabaey of UC Berkeley.

Four papers will be presented in each of the 12 sessions:

1. Energy Reduction in Processor Pipelines
2. Voltage and Instruction Scheduling
3. Low Power RF Circuits and Systems

4. Modeling and Estimation Techniques
5. Low Power Digital Circuits
6. Bus Encoding
7. Technology for Low Power
8. Architectural Techniques
9. Low Power Analog Techniques
10. Algorithmic Transformations and Caching
11. Low Power Digital Building Blocks
12. Power Supply and Delivery

Poster sessions, after the last morning session and continuing through lunch, allow an opportunity to survey more late-breaking news on designing low-power electronic systems. Invited speakers are fea-

tured each day as the first session in the afternoon:

- “Cooling and power considerations for semiconductors into the next century,” Christian Belady, Hewlett Packard
- “Wireless sensor networks: Application driver for low power distributed systems,” Deborah Estrin, UCLA

To see more details of the advance program, browse [www.cse.psu.edu/~islped](http://www.cse.psu.edu/~islped).

Advance symposium registration rates end 1 July 2001 at [campus.acm.org/register/islped01/](http://campus.acm.org/register/islped01/)

Before 13 July, event rates at the hotel are available for registrants. Tel: +1 714 960 7873. ●

## SSCTC Workshop on Low-Power Circuits

11–12 October 2001

Key Bridge Marriott Hotel,  
Arlington, VA

SSCTC workshops are interactive meetings of experts in disciplines related to IC design and similar topics. The number of attendees is limited to promote good communication between speakers and attendees. The workshops are neither tutorials nor short courses; they are informal, and there are no written presentations. Attendees are active in the field of the workshop. The speakers discuss the latest developments in their work, and there is ample time allocated for audience participation and discussion.

Mark your calendar and check [www.ieee.org/ssctc](http://www.ieee.org/ssctc) for speaker and registration details.

### President:

Bruce Wooley  
Stanford University  
Stanford, CA  
wooley@ee.stanford.edu  
Fax: +1 650 725 3383

### Vice President:

Charles G. Sodini  
Massachusetts Institute of Technology  
Cambridge, MA

### Secretary:

Asad Abidi  
University of California  
Los Angeles, CA

### Treasurer:

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### Newsletter Editor:

Lewis M. Terman  
IBM Research  
Yorktown Heights, NY  
terman@us.ibm.com  
Fax: +1 914 945 1358

For detailed contact information, see the Society Web page: [www.sscs.org/info/](http://www.sscs.org/info/)

For questions regarding Society business, contact the SCS Executive Office.

Contributions for the July issue of the newsletter **must be received by 1 August 2001** at the SCS Executive Office.

Anne O'Neill, Executive Director  
IEEE SCS  
445 Hoes Lane, P.O. Box 1331  
Piscataway, NJ 08855-1331

Tel: +1 732 981 3400  
Fax: +1 732 981 3401  
Email: [sscs@ieee.org](mailto:sscs@ieee.org)

# BiCMOS and BiFET Integrated Circuits Engineers to Meet at BCTM

The 2001 Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) will be held in Minneapolis, MN from 30 September to 2 October 2001. BCTM provides a forum for technical communication focused on the needs and interests of bipolar and BiCMOS engineers. The conference covers the design, performance, fabrication, testing, and application of bipolar, BiCMOS, and BiFET integrated circuits. This year's conference includes a Short Course, an evening banquet, several invited papers, a vendor exhibition, and a Best Student Paper award.

The conference will begin with a Short Course on Sunday, 30 September. The course is divided into four 1.5-hour sessions. The first session will be taught by Klaus Runge (Gtran) covering high-speed IC circuit design for optical communications. Joerg Berkner (Infineon Technologies AG) will teach the second session and will discuss parameter extraction for bipolar compact models. The third session will be led by Jeff Johnson (IBM) on the topic of industrial experience with SiGe HBT simulation — from process to compact models without running a wafer in fab. David Pehlke (Ericsson) will give the final Short Course session on the subject of production RF measurement techniques. The BCTM Short Course has become a very popular part of the conference and attracts a large percentage of the BCTM attendees each year.

On Monday morning, the technical program begins with the keynote speaker, Behrooz Abdi (Motorola). Mr. Behrooz will discuss communication applications for the next decade and their requirements for circuits and technologies. After the Monday morning technical sessions, the attendees are invited to a luncheon. This year's luncheon speaker will be Isaac Chuang from MIT Media Lab. A banquet will be held on Monday evening. Several exhibits by design, test/measurement, and CAD/modeling vendors will be on display at the conference.

The conference technical sessions offer exceptional technical papers that provide the latest and most significant developments in Bipolar/BiCMOS integrated circuits. Invited and tutorial papers by leading experts from industry and academia highlight the technical sessions. These papers focus on new directions in Bipolar/BiCMOS technology, including emerging technologies. Look for the advance program at [www.ectm.et.tudelft.nl/](http://www.ectm.et.tudelft.nl/) [www/BCTM](http://www/BCTM). Major topics include:

- Analog/Digital Design
- Radio Frequency Design
- Device Physics
- Modeling and Simulations
- Process Technology
- Power Devices: Discrete and Integrated Bipolar/ BiCMOS Power Devices and High-Voltage ICs

The Bipolar/BiCMOS Circuits and Technology Meeting will be held at the Marriott City Center Hotel in downtown Minneapolis. The Marriott offers the finest hotel accommodations in the Twin Cities area and is central to the ultramodern City Center shopping complex, the skywalk to Nicollet Mall, and Minneapolis cultural attractions such as the Guthrie Theater, Minneapolis Orchestra Hall, and the historic Orpheum and State theaters. In nearby Bloomington is the largest fully enclosed retail and family entertainment complex in the United States: The Mall of America. There are two wonderful zoos and many other tourist attractions in the Twin Cities area.

BCTM is sponsored by the IEEE Electron Devices Society, in cooperation with IEEE Solid-State Circuits Society and the IEEE Twin Cities Section. The 2001 Conference Chair is Kenneth O, University of Florida, Gainesville, and the Technical Program Chair is Hiroshi Iwai, Tokyo Institute of Technology, Yokohama, Japan.

To register, use the forms available online at [www.ectm.et.tudelft.nl/www/BCTM](http://www.ectm.et.tudelft.nl/www/BCTM).

For additional information, contact the BCTM Conference Manager, Janice Jopke, CCS Associates. Email: [prairie66@qwest.net](mailto:prairie66@qwest.net). ●

## Tom Skaar

*BCTM Publicity Chairman*  
[tskaar@vitesse.com](mailto:tskaar@vitesse.com)

## SSCS Cooperates to Announce: Events of Topical and Regional Interest to Our Members

The following are events of topical and/or regional interest to our members.  
Also posted on [www.sscs.org/meetings](http://www.sscs.org/meetings)

**MTDT 2001 IEEE International Workshop on Memory Technology, Design and Testing**  
6–7 August 2001, San Jose, CA,  
Deadline: passed  
[r.rajsuman@advantest.com](mailto:r.rajsuman@advantest.com)

**MIEL 2002 23rd International Conference on Microelectronics**  
12–15 May 2002, University of Nis, Yugoslavia, Deadline: 30 September 2001  
[europa.elfak.ni.ac.yu/miel/](mailto:europa.elfak.ni.ac.yu/miel/)

**EDM '2002 3rd Siberian Russian Workshop and Tutorial on Electron Devices and Materials**  
5–9 July 2002, Novosibirsk State Technical University, Russia, Deadline: 30 March 2002  
[www.ref.nstu.ru/ieeesb/edm](http://www.ref.nstu.ru/ieeesb/edm)

# European Solid-State Circuit Conference— ESSCIRC 2001 Preview

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The 27th ESSCIRC will take place 18–20 September 2001 in Villach, Austria.

Villach is the major center of microelectronics in Austria, where Infineon runs a design center with 360 employees and a wafer fab with more than 2400 employees. Only 1.5 hours away by car is Austria's second microelectronics company, Austria Mikro Systeme.

Villach is a charming old town with Mediterranean flair, surrounded by a vacation area of clear bathing lakes, traditional thermal baths, and numerous summer and winter sport resorts. It is the ideal backdrop for a successful event.

ESSCIRC 2001 will have 104 papers in three parallel sessions, covering RF, analog, mixed signal and digital circuits, A/D and D/A converters, opto electronics, Systems-On-A-Chip, and IP blocks.

Invited speakers will present their views on hot topics in microelectronics:

“SoC design from a mixed signal perspective,” Willy Sansen, Katholieke Universiteit Leuven, Belgium

“Mixed signal service and foundry—a business model for the future?” Wolfgang Pribyl, Austria Mikro Systeme, Austria

“Microelectronics for home entertainment,” Yoshi Hagiwara, Sony, Japan

“Trends and challenges in VLSI technology scaling towards 100 nm,” Stefan Rusu, Intel, USA

“Integrated circuits for the next generation wireless system,” Josef Hausner, Infineon, Germany

“Communication busses for automotive applications,” Stefan Poledna, TTTech, Austria

“Automated processor generation for system-on-chip,” Chris Rowen, Tensilica, USA

“MEMS components for reconfigurable RF interfaces,” A. Kaiser, IEMN-ISEN, France

On Monday, 17 September, a workshop focusing on System-On-A-Chip/Systems in Packages will be given by H. Tenhunen, KTH, Sweden; M. Steyart, KUL, Belgium; and J. Huisken, Philips, The Netherlands.

On Friday, 21 September, a tutorial will be given on Smart Power, X-by-Wire, Body Electronics, and Communications Electronics in the Automotive Environment.

Further information about ESSCIRC 2001 can be found at [www.esscirc.org/esscirc2001](http://www.esscirc.org/esscirc2001). ●

## **Herbert Grünbacher**

*General Chairman*  
Carinthia Technical Institute

## **Franz Dielacher**

*Program Chairman*  
Infineon

# Looking Back on the 2001 VLSI-TSA

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The 2001 International Symposium on VLSI Technology, Systems, and Applications was held 18–20 April in Hsinchu, Taiwan. The objective of the conference was to bring together scientists and engineers from all over the world who are actively engaged in research and development of VLSI technology, systems, and applications, to discuss current progress in this field with the experts from Taiwan's local industry. There were two main changes made by the organizing committee: shifting the meeting from the traditional June time frame to take advantage of the beautiful spring season in Taiwan and moving the conference location from Taipei to Hsinchu, the center of advanced integrated circuit design and manufacturing in Taiwan. This year's meet-

ing attracted more than 600 attendees, a substantial increase over previous years and a strong indication of success, particularly considering the current economical climate.

## **Highlights of Keynote Speeches**

Three keynote speeches were delivered by leading thinkers from the United States, Europe, and Japan to position the theme of the 2001 VLSI-TSA on systems and complexities. The scaling of silicon technology provides the possibility of creating complete systems on one integrated circuit chip. In “Systems on a chip from a system's perspective,” Gene Frantz (Senior Fellow, Texas Instruments, USA) discussed the why, when, and who of Systems-On-A-Chip to dramatically improve system-level performance, cost, and

power. In “Future is in wireless,” Jari Pasanen (Vice President Research and Technology Access, Nokia, Finland) detailed how wireless terminal manufacturers address the various design challenges in RF and baseband to ensure fast product creation with rapidly increasing system complexity in the Third Generation mobile communications systems for wireless Internet. Toyoki Takemoto (Executive Vice President, STARC, Japan) described the promotion of industrial/academic joint projects and precompetitive R&D activities on circuits and systems in “Joint activity for semiconductor R&D and role of Semiconductor Technology Academic Research Center (STARC).”

*Continued on next page*

### Technical Programs

In addition to the keynote presentations, the technical sessions featured two parallel tracks; one on Technology and the other on Circuits and Applications. With the 14 invited papers as the backbone setting the stage for technical interactions, the main contents of VLSI-TSA were the 66 contributed papers, selected from about 120 excellent submissions from all over the world, representing original works on the latest advances in the area of VLSI technology, circuits, and applications.

### Highlights of Technology Sessions

The Technology track consists of five sessions on the topics of device technology and reliability, DRAM, RF and System-On-A-Chip technology, gate dielectrics, and interconnects. There were a total of six invited papers and 33 contributed papers.

In the Device Technology session, G. Shahidi from IBM gave a review of SOI technology. Shahidi's theme was that SOI development is driven by high-end microprocessors, but it will benefit many other applications, such as RF and low power. B. Mizuno of Matsuhita Electric described the need for and challenge of ultra-shallow junctions. An approach to ultra-shallow junctions is by plasma doping followed by RTA or laser anneal.

In the DRAM session, K. Kim from Samsung reviewed the status of 1T1C FRAM technology. Recent progress suggests that FRAM with a cell size of  $10F^2$  can be realized, making FRAM within a factor of two of DRAM in cell size. Other highlights included a paper describing a  $6F^2$  DRAM cell in  $0.13\text{-}\mu\text{m}$  technology. Another paper showed that CMOS devices in an embedded DRAM technology can have the same performance as CMOS devices in a logic technology of the same lithography generation.

The RF and System-On-A-Chip Technology session featured two



**Dr. Tak Ning, Symposium Chair, at the opening session.**

invited papers, one by D. Bishop of Lucent Technologies on the role of MEMS in optical communications and one by J. Burghartz of Delft University of Technology on tailoring logic CMOS devices for RF applications. With some care, CMOS logic devices can be very good for RF applications.

High-K gate dielectric is a hot research topic. Most of the papers in the gate dielectric session dealt with high-k gate dielectrics, including an invited paper by M. Houssa from the Katholieke Universiteit Leuven, which reviewed the electrical and physical characteristics of high-K dielectrics.

Highlights of the Interconnect session included a paper from TSMC on using the stress current to raise the temperature of the metal lines being tested for electromigration. The method reduces the time needed for test and feedback in the development process.

### Highlights of Circuits and Applications Sessions

The Circuits and Applications track consisted of four short sessions on wireless, networking ICs, communication ICs, and mixed signals; and three long sessions on multimedia processing, specialized circuit techniques, and logic circuits. There were a total of eight invited papers and 30 contributed papers from seven countries. About 40% of

the papers were from the United States, and 37% were from Taiwan.

Bob Brodersen of UC Berkeley gave an invited talk on Wireless System-on-a-Chip (SOC) Design. Brodersen used wireless systems as an example of System-On-A-Chip, which is better positioned to exploit parallelism inherent in the application. This opportunity can lead to a more hardware-dominated solution that offers much better efficiency in power, area, and performance. In this session, a paper from Conexant Systems described a WCDMA receiver design, and a paper from Chiao-Tung University revealed an early-late gate scheme for Bluetooth packet receiving that eliminates the use of ADC.

Joseph Williams of Bell Laboratories started the Networking ICs session with an invited talk on the architectures for networking processing. The talk described a survey and analysis of architecture features shared among commercial network processors that perform packet processing via the flexibility of a microprocessor, but with the performance of a dedicated ASIC. A paper from Bell Labs described simple link protocol for zero-overhead high-speed Ethernet packet delineation. Three papers from Taiwan covered circuits for k-WTA/sorting network, routing switch design for irregular interconnect network, and an RFIC for a DCS 1800 base station receiver downconverter.

The Communication ICs session featured an invited paper from K. Azadet of Bell Labs describing the main challenge in 1000 BASE-T Gigabit Ethernet: DSP implementation. A paper by Yu et al. from UCLA and Bell Labs demonstrated a 38% power savings in a FIR filter design by using a novel number presentation that avoids MSBs switching. Another Bell Labs paper described a 2X throughput design of 14-tap PDFD for 1000 BASE-T Gigabit Ethernet.

Josef Fenk of Infineon delivered the invited paper for the Mixed Sig-

nal session. Fenk gave a status review and development trend for digital cellular and cordless system, which demands highly integrated RF ICs for GSM, DECT, and UMTS. Tiew et al. from the U.K. described a design of a sixth-order MASH DS modulator. Huang et al. from Taiwan presented a cost-effective design binary FSK demodulator that eliminates the need for a postdetection filter.

The Multimedia Processing session featured A. Theuwissen of Philips as an invited speaker on comparison of CCD and CMOS image sensors. Theuwissen analyzed the reason for better CCD image quality and predicted future trends. Another invited paper by Paul Stravers of Philips Research argued the drive for chip-level homogeneous multiprocessing implementation for multimedia processing. Three papers described various aspects of MPEG and JPEG designs. Samsung presented S3C4520X, a System-On-A-Chip system manager for network applications. Winbond presented another System-On-A-Chip for an analog

and digital record, playback, and processing system.

The Specialized Circuit techniques session covered innovations on ESD protection, low-noise amplifiers, low-voltage charge pumps, a single-chip Intelligent Power Module, and a programmable BIST scheme.

In the Logic Circuits session, O. Takahashi of IBM Research delivered an invited paper for Sang Dhong on power-conscious circuit design techniques for high-performance processors. Cary Chin of Sun Microsystems delivered the other invited paper for Ward Vercysee on CAD methodology challenges fueled by a fast-paced increase in microprocessor design complexity and performance. The session also featured several SOI design techniques from IBM, a systolic multiplier, an efficient inversion and division unit, and a level shifter design for 0.13- $\mu\text{m}$  technology.

#### Other Conference Highlights

The VLSI-TSA also provided a forum for the recognition of individuals who have made outstanding contributions to the progress and

development of the VLSI industry in Taiwan. This year, three individuals were recognized at the plenary session on 18 April. They were Dr. Bob O. Evans, Managing Partner at Technology Strategies and Alliances and a Partner in Rocket Ventures; Dr. Genda J. Hu, Vice President of Advanced Technology Development at TSMC; and Dr. Ding-Yuan Yang, Vice Chairman of Winbond Electronics Corporation.

The International Symposium on VLSI Technology, Systems, and Applications is held every other year. For information on the 2003 conference, look on the conference website, [www.erso.itri.org.tw/vlsi-tsa](http://www.erso.itri.org.tw/vlsi-tsa), starting in early 2002.

Presentation slides for the 2001 conference are available on the conference website. *The Proceedings of Technical Papers of 2001 International Symposium on VLSI Technology, Systems, and Applications* can be purchased either by contacting the conference secretariat ([annieleee@itri.org.tw](mailto:annieleee@itri.org.tw)) or through the IEEE (IEEE Catalog Number: 01TH8517). ●

## In Memory of Peter Verhofstadt



**Peter Verhofstadt**

Peter Verhofstadt, a close friend and colleague of many of us in the solid-state circuits community, passed away on May 10, 2001, after a long battle with cancer. Peter contributed enormously to solid-state circuits community. In the 1970s he was an early pioneer in areas such as semiconductor memory, digital signal processing and computer-aided design. In 1991 he joined the SRC and subsequently played a very

significant role in shaping the structure of research support for microelectronics. For example, the SRC Focus Center Research Program is largely his creation.

Among his many professional contributions, Peter served as President of the Solid-State Circuits Council; a guest editor of the *Journal of Solid-State Circuits*; and Chair of the ISSCC, the Solid-State Circuits and Technology Committee, and the VLSI Circuits Symposium. He was also one of the founders of the Symposium on Low Power Electronics, and he served the Solid-State Circuits Society in a variety of capacities. The entire community will miss his extraordinary insight and dedication, as well as his warm and gracious personality.

Peter is survived by his wife Betty, children Kirsten and Derek, and grandson Nicolas. Condolences may be sent to the family at 18691 Casablanca Avenue, Saratoga, CA 95070. ●

#### **Bruce Wooley**

*SSCS President*

[wooley@par.stanford.edu](mailto:wooley@par.stanford.edu)

## SSCS Members Honored as 2001 IEEE Fellows

**M. Omair Ahmad**

**Concordia University,  
Montreal, Quebec, Canada**

*For contributions to the design and implementation of digital signal processing algorithms.*

**H. Jonathan Chao**

**Polytechnic University, Brooklyn, NY**

*For contributions to the architecture and application of VLSI circuits in high speed packet networks.*

**Liang-Gee Chen**

**National Taiwan University,  
Taipei, Taiwan**

*For contributions to algorithm and architecture design for video coding systems.*

**John D. Cressler**

**Auburn University, Auburn, AL**

*For contributions to the understanding and optimization of silicon and silicon-germanium bipolar transistors.*

**Evan Ezra Davidson**

**IBM Corporation,  
Hopewell Junction, NY**

*For contributions and leadership in the fields of signal integrity and noise control in digital systems.*

**Geert Adolf De Veirman**

**Texas Instruments, Tustin, CA**

*For contributions to the design of continuous-time filters and hard-disk drive read channel ICs.*

**Yoshiaki Daimon Hagiwara**

**Sony Corporation, Tokyo, Japan**

*For pioneering work on, and development of, solid-state imagers.*

**Hiroshi Ishiwara**

**Tokyo Institute of Technology,  
Yokohama, Japan**

*For contributions to Si-based heterostructure devices and ferroelectric memories.*

**David Andrew Johns**

**University of Toronto,  
Toronto, Ontario Canada**

*For contributions to the theory and design of analog adaptive integrated circuits used in digital communications.*

**Daniel J. Kenneally**

**Consultant, Rome, NY**

*For contributions to the development and practice of computer-aided modeling, simulation, and diagnostics of electromagnetic interference effects on integrated circuits and multichip modules.*

**Robert Forrest Kwasnick**

**General Electric Medical Systems,  
Perkin-Elmer Amorphous Silicon,  
Santa Clara, CA**

*For contributions to the development of amorphous silicon flat panel x-ray imager technology.*

**Parag Kumar Lala**

**University of Arkansas,  
Fayetteville, AR**

*For contributions to the development of self-checking logic and associated checker design.*

**Richard Webster Linderman**

**Air Force Research Laboratory,  
Rome, NY**

*For contributions to the design of embedded high performance computing technology and its use in aerospace signal and image processing systems.*

**Kenji Nishi**

**Semiconductor Leading Edge  
Technologies, Inc.,  
Yokohama, Kanagawa, Japan**

*For contributions to semiconductor  
process and device modeling and  
the development of software for  
their simulation.*

**Massoud Pedram**

**University of Southern California,  
Los Angeles, CA**

*For contributions to the theory  
and practice of low-power design  
and CAD.*

**John Xavier Przybysz**

**Northrop Grumman Corporation,  
Baltimore, MD**

*For contributions in the development and  
application of Josephson digital circuits  
to electronic systems, especially radars,  
communication satellites, and data  
switching networks.*

**Krishna Shenai**

**University of Illinois, Chicago, IL**

*For contributions to the design of  
high-speed silicon and silicon/  
germanium bipolar circuits, especially  
as applied to fiber-optic systems.*

**Bertram Emil Shi**

**Hong Kong University of Science  
and Technology, Clear Water Bay,  
Kowloon, Hong Kong**

*For contributions to the analysis,  
implementation, and application of  
cellular neural networks.*

**Ritu Shrivastava**

**Alliance Semiconductor Corporation,  
Santa Clara, CA**

*For contributions to high-performance  
CMOS memory technology and  
product development.*

**James C. Sturm**

**Princeton University, Princeton, NJ**  
*For contributions to novel silicon-  
based semiconductor devices and  
large-area electronics.*

**Christofer Toumazou**

**Imperial College, London, U.K.**

*For contributions to the field of analog  
circuit design with particular emphasis  
on current-mode signal processing.*

**Yang Yuan Wang**

**Peking University, Beijing, China**

*For leadership in China's semiconductor  
research and education.*

**Hon-Sum Philip Wong**

**IBM T. J. Watson Research Center,  
Yorktown Heights, NY**

*For contributions to solid-state image  
sensors and nanoscale CMOS devices.*

In addition to the nine evaluated by the Solid-State Circuits Society who were profiled in April's newsletter, here are 23 more members of SSSC who are now Fellows. The IEEE conferred the distinction of Fellow on 249 of its class of 2001.

An IEEE Fellow is a member of unusual distinction in the profession. It is a recognition conferred only by invitation of the Board of Directors on a person of extraordinary qualifications and experience in the IEEE fields of interest, who has made important individual contributions to one or more of these fields. No more than one tenth of one percent of the total Institute membership may be advanced to Fellow grade in any given year.

A nominee must be a Senior Member of the Institute and have been a member in any grade for at least five years prior to the year of election. A nomination for Fellow and references must be submitted by mid-March each year. Begin planning for 2002 by applying for election to Senior grade at [www.ieee.org/membership/upgrade.html](http://www.ieee.org/membership/upgrade.html).

# Chapter News

## SSCS Chapters Chairs Confer

Fu Li, IEEE Region 6 Chapter Coordinator, spoke at the third annual SSCS lunch for Chapter Chairs held during the ISSCC. Attending were 20 representatives from SSCS chapters and five additional SSCS AdCom leaders. Li's presentation was timely, as the third week of February is the deadline for chapters and sections to report their activities to the IEEE Regional Activities office. He reminded chapters that their L31 meeting reports are used to determine financial rebates to sections. All chapters are allocated \$180 through their IEEE sections. Chapters were reminded to request those funds from their sections to help with events and projects.

Seven chapters presented highlights of their year-long activities; Japan, Korea, Dallas, Ireland, Shariff University Student Chapter, Toronto, and Taiwan. Activities organized by chapters included:

- workshops and conferences
- student awards
- short courses
- websites
- support and participation of local industry
- presentations by SSCS Distinguished Lecturers and local experts
- presentations of highlights from noteworthy conferences

## New Distinguished Lecturers

Since the Chapters Chairs meeting in February, three new Distinguished Lecturers have been named: Vojin G. Oklobdzija of UC Davis, Dick Hester of Texas Instruments, and Massoud Pedram of UCLA. SSCS Distinguished Lecturers have recently been hosted by the University of Michigan; Polytechnic of Catalunya, Barcelona, Spain; TIMA Laboratory, Grenoble, France; and chapter meetings in Toronto and Montreal. Details of Distinguished Lecture topics are online at [www.sscs.org/DL](http://www.sscs.org/DL) or by autoretrievable email from [info.distlec.ssc@ieee.org](mailto:info.distlec.ssc@ieee.org).

## Joint ED/SSC Student Chapter Establishment at the University of Tehran: A Step Toward Integrity

**Ali Khakifirooz, Interim Chair, ED/SSC Student Chapter**  
[khaki@mtl.mit.edu](mailto:khaki@mtl.mit.edu)

Established in 1996, the University of Tehran's IEEE Student Chapter has played a major role in introducing the Institute's premier goals to Iranian academics. Our student branch has held a number of successful workshops alongside the normal activities, and this has led to enthusiasm among the students to arrange such activities in student chapters. We also had weekly seminars on microelectronics presented by graduate students and faculty members and were honored to

have several excellent lectures by Prof. Kenneth R. Laker (former president, IEEE), Prof. M. Pedram of USC, Dr. G. G. Shahidi of IBM, Prof. A. Hajimiri of Caltech, Profs. A. Nathan and M. I. Elmasry of U. Waterloo, Prof. J. D. Meindl of Georgia Tech, and Dr. F. Assaderaghi of IBM. One of the main programs that motivated our branch to establish a joint ED/SSC Student Chapter was the involvement of branch members in organizing the 12th International Conference on Microelectronics (ICM 2000), technically cosponsored by the EDS.

In addition to the students' interest, the impressive quality of the research being conducted in our labs has developed an atmosphere in which every individual is encouraged to contribute ideas. Establishing a student chapter simply directs such contributions and lets us gain experience from our peers worldwide and to share our experiences with them.

We know that the first year of a student branch is very critical to its development. Therefore, we have a detailed plan to continue our weekly seminars, to start research projects for undergraduate students, to coorganize the 4th Iranian Student Conference on Electrical Engineering (ISCEE'01), to increase the technical knowledge of the students by presenting conference videotapes and web casts, to plan Distinguished Lecturers programs, and to start a promotional campaign to recruit new Society members. I would like to thank the faculty



**Chairs of SSCS chapters from the head of the table clockwise: Jan Van der Spiegel (Chair of the Chapters Committee), Christer Svensson (Chair of the Distinguished Lectures Program), next to the waiter is Dr. Katsuro Sasaki (Vice Chair of Japan Chapter), Dr. Tsuneo Tsukahara (Treasurer of Japan Chapter), Moon Key Lee (Chair of Seoul Chapter), Kwang Sun Yoon (Secretary of Seoul Chapter), Michael Peter Kennedy (Chair of Ireland Chapter), and facing the camera is Zhihua Wang (Chair of Beijing Chapter). Standing in profile and greeting a Chapter Chair is SSCS President Bruce Wooley.**

and my friends who made this possible, and I am looking forward to their continued support. I would also like to acknowledge the invaluable support and encouragement of EDS and SSCS Chapter Chairs and officers.

Special thanks goes to our Chapter Vice Chair, Ms. Mahnaz Maddah, who is managing the activities during my leave of absence at MIT.



**Board members of the SSCS Germany Chapter met on 2 February 2001 during the 25th Multi Project Chip Workshop in Aachen, Germany. (l-r) Prof. W. Bonath (Treasurer), Dr. K. Ayadi (Educational Activities), Dr. H. Blume (Chair), and Prof. Dr. K. Schmidt (Vice Chair).**

### Dallas Meetings

Spring 2001 speakers at the Dallas Chapter included Dr. Paul Yu, "A 14b 40MSample/s pipelined ADC with DFCA," and Jan Van der Spiegel, "Biologically inspired vision sensors." Using the CD recording of the ISSCC 2000 Short Course at one chapter meeting, attendees listened to one of the conference speakers, Dr. Allen Podell, speak on "The lowdown on low noise amplifiers."

### Germany Chapter Holger Blume, Chapter Chair blume@eecs.rwth-aachen.de

Just starting its second year, the SSCS Germany Chapter is developing programs to serve its membership. In the winter of 2000, inspired by Prof. Dr. R. Jansen, the former Chair of the IEEE Germany Section, Holger Blume, senior engineer of

the Electrical Engineering and Computer Systems (EECS) Department at Aachen Institute of Technology, RWTH Aachen, invited the 550 members of the Solid-State Circuits Society in Germany to participate in forming the first German SSCS chapter. Officers of the Chapter now come from many regions of Germany and different academic institutions and companies.

In its first year, the Germany Chapter started several activities. A weekly series of lectures and presentations entitled VLSI Architecture for Digital Signal Processing took place at the Aachen Institute of Technology. Organized by Holger Blume and Tobias Noll (Chair of the EECS Department), the series has included outstanding contributions by, for example:

- "Challenges in the 21st century

digital signal processing," Prof. L. Gazsi, Infineon AG Dusseldorf

- "Advances in consumer video format conversion," Prof. G. de Haan, Philips National Laboratory and TU Eindhoven
- "HF-CMOS circuits for wireless communication," Prof. H. Klar, TU Berlin
- "Hiperlan II — architecture concepts for base band signal processing," Dr. T. Herfet, Grundig AG Nürnberg
- "Models and methods for the integration of heterogeneous hardware and software components," Prof. L. Thiele, ETH Zürich

Students of RWTH Aachen have participated in several excursions organized through the Chapter to semiconductor companies such as Infineon, Mitsubishi, and Nokia.

In February, Prof. Dr. K. Schmidt from the University of Applied Sciences in Furtwangen (Chapter Vice Chair) and Prof. Dr. K. Bonath from the University of Applied Sciences Giessen (Chapter Treasurer) co-organized the 25th Multi Project Chip Workshop in Baden-Württemberg. This semiannual workshop is now a cooperative event of the SSCS Chapter and the MPC (Multi-Project-Chip Group). ●

## Profile: Aachen Institute of Technology, RWTH (Rhine Westphalia)

The Electrical Engineering and Computer Science (EECS) Department of RWTH Aachen, Germany, chaired by Prof. Dr. Tobias G. Noll, has three fundamental research domains: physical oriented VLSI design methodologies, VLSI architectures and circuits for digital signal processing, and digital signal processing in medical electronics.

An important outcome of the

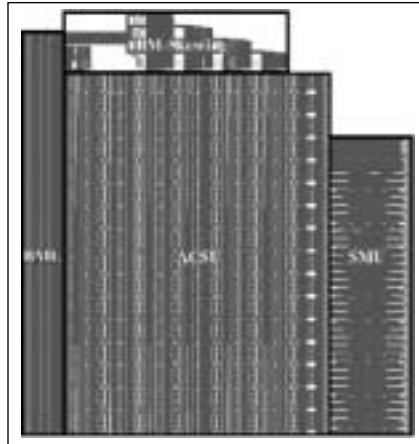
research on design methodologies is the prototype implementation of a data path generator (DPG) tool. Starting from a high-level description of the signal flow graph (SFG) to be implemented, this tool automatically assembles highly optimized hard macro layouts from a set of abutment cells. These abutment cells again are automatically derived from a small library of predesigned optimized leaf

cells. This approach exploits the inherent regularity and locality typically associated with SFGs of digital signal processing for superior features in throughput rate, silicon area, and even more important, power dissipation. It offers the possibility of iterative optimization of the SFG by simply modifying the SFG description, it supports the implementation

*Continued on next page*

of parameterized generic SFGs for frequently used building blocks such as IP blocks, and it can also be applied as a generator that is simple to use in dedicated macro generation. The tool is not limited to arithmetic data paths, but also allows the implementation of highly efficient building blocks such as customized memory macros. It is integrated into an industrial standard design framework and combines the advantages and flexibility of physical oriented design with short design times comparable to today's synthesis-based high-performance designs. (For detailed information, see [www.eecs.rwth-aachen.de/dpg/info.html](http://www.eecs.rwth-aachen.de/dpg/info.html).)

Research highlights from the VLSI architectures and circuits activities demonstrate the strengths of physical oriented design: A Viterbi Decoder for hard disk read/write channel applications was designed for a symbol rate of 550 Msymbols/sec, consuming about 500 mW on less than 1 mm<sup>2</sup> in a 0.25- $\mu$ m CMOS technology. The overall design effort from scratch to the verified hard macro, characterized by all views required in the design framework, was as small as 3 man-months. For video broadcast applications, another Viterbi Decoder was implemented in a 0.35- $\mu$ m CMOS technology. Operating at



**A 550 Mb/s Radix-4 Bit-Level Pipelined 16-State 0.25- $\mu$ m CMOS Viterbi Decoder.**

90 MHz, the decoder's power dissipation of only 120 mW outshines other recently published realizations of the same specification in comparable technologies.

For application in handheld ultrasound scanners, a digital beam-former chip is currently being developed in cooperation with Pie Medical, Maastricht, The Netherlands and Fraunhofer Institute IMS, Duisburg, Germany. The cardinal goal of that design experiment, which is funded by the European Commission, is the lowest possible power consumption that allows long-time battery operation of the system.

A rather new activity targets for highly efficient reconfigurable hetero-

geneous architectures for challenging single-chip signal-processing systems. In cooperation with the industrial partner Sony, implementation cost models are elaborated that support the partitioning of such systems. The implementation alternatives considered include DSP kernels, reconfigurable (FPGA-like) arrays, and dedicated macro blocks. Such heterogeneous architectures will be required in the future to fulfill the many-fold requirements of future Systems-On-A-Chip; for example, for flexibility (i.e., programmability and/or reconfigurability) for the highest computational power with a small silicon area and especially for power dissipation.

Concerning international studies at RWTH Aachen, the EECS Department of the Aachen Institute of Technology is coordinating a master's degree program in computer engineering for students from foreign countries already holding a bachelor's degree. Therefore, the EECS Department is interested in obtaining information about the research focus of academic institutions of other SSCS chapters in Europe, especially in Eastern Europe and countries of the former Soviet Union. Cooperative research and the establishment of cooperation for student exchange are most welcome here. ●

## ISSCC 2001 Panel Discussion: Has Technology Scaling Created Microprocessor Monsters?

Process engineers have provided generation after generation of CMOS technologies that somehow continue to fulfill Moore's Law. Architects have shrewdly exploited this capability with innovative schemes that increase parallelism and pipeline depth, change instruction execution order, and drive more speculative operations. These techniques have improved architectural performance at the expense of power, die size, and complexity. Our panelists shared very polarized opinions on whether these boundary conditions and their trends were

sustainable and remained practical or if alternative design paradigms are becoming apparent.

The Patterson-Hennessy Equation indicates the time required to complete a transaction may be enhanced by improving (1) the number of instructions the chip can retire per cycle, (2) the number of cycles required per instruction, or (3) the number of seconds the machine consumes per cycle. David Harris, Assistant Professor of Engineering at Harvey Mudd College, argued that because of diminishing returns in architecture performance, it was

more profitable to spend resources on high-performance circuits rather than on increasing architectural overhead [item (3) above]. He also noted that increased exposure to noise and skew identified selected circuit topologies, such as skew-tolerant domino, as being "best fits" in future chips.

Kazuo Yano, Senior Researcher at Hitachi's Central Research Laboratory, countered that a mix of circuit styles, each well suited to a given function, will be found on successful microprocessors of the future. He added that each of these styles

will also thrive with selected technology features to enable them.

Perhaps even more outspoken, but with a similar outlook, Bob Montoye, Research Staff Member at IBM's Austin Research Laboratory, described the circuit design "dark age" that aggressive architectures and technology worship have created. He argued for designing to the original simpler metrics of latency and bandwidth.

On the other end of the spectrum, Yale Patt, Professor of Electrical and Computer Engineering at the University of Texas, reminded the audience that the design community has indeed coped well with the complexity and device count that contemporary architectures have conjured up. Prof. Patt believes that the innovation and creativity bringing the industry to this point will continue to deliver

solutions that manage complexity.

David Patterson, Pardee Professor of Computer Science at the University of California, Berkeley, encouraged the audience to look beyond the present paradigm in stand-alone processors. By paying close attention to predominant functions required, Prof. Patterson believes substantial underutilized capability exists in the embedded space and in the server market. Each, he argued, drives specific requirements, which when customized can produce superior throughput.

Ruby Lee, Hamrick Professor of Electrical Engineering at Princeton University, extended this concept of customizing compute resource to the task. Prof. Lee argued that programmable processors, scalable power and clock cycle, and dynamically reconfigurable machine

instruction sets are critical to producing chips with performance and power characteristics well suited to a multiplicity of market applications.

Audience participation highlighted the industry awareness of the baggage carried by these complex architectures. Array multiprocessing, possibly using simpler, lower power microprocessors, will clearly be a relief to the design community, but it is gated by the development of applications and compilers that have figured out how to harness this computing capability via job partitioning. ●



**Kerry Bernstein**  
IBM Burlington, VT  
kbernste@us.ibm.com

## 2002 International Conference on Microelectronics (MIEL 2002)

The International Conference on Microelectronics (MIEL) is a major European conference that provides an international forum for the presentation and discussion of the recent developments and future trends in the field of microelectronics. Since 1984, an aura of internationalization has surrounded the MIEL conference, providing an opportunity for specialists from both academic and industrial environments in the West and East, as well as from the countries of the Third World, to meet in an informal, friendly atmosphere and to exchange experiences in the theory and practice of microelectronics.

The 23rd MIEL will be held 12–15 May 2002 at the Faculty of Electronic Engineering, University of Nis, Yugoslavia. The topics to be covered include all important aspects of microelectronic devices, circuits and systems, technologies and devices, device physics and modeling, process and device simulation, circuit design and testing, system design and packaging, and charac-

terization and reliability. Based on data from the conference over the past decade, MIEL 2002's program is expected to consist of about 150 contributed papers by the leading authorities from more than 30 countries, structured into oral and poster sessions, plus 15 invited papers. Two workshops, Power Devices and ICs and Microsystem Technologies, of six invited papers each, will round out the technical program of the conference.

Among the invited papers are:

- "Process-related reliability of gate dielectric for ULSI device," C.Y. Chang, National Chiao Tung University, Taiwan
- "Isolation issues in power integrated circuits," G. Charitat, LAAS-CNRS, France
- "SOI devices for 0.1 micron gate lengths," J.-P. Colinge, University of California, USA
- "Access to microsystem technology: The MPC services solution," B. Courtois, CMP, France
- "Microsystems: Research task,

education task, application fields, examples," H. Dettner, Technical University of Vienna, Austria

- "Silicon carbide parameters for process and device CAD tools," S. Dimitrijevic, Griffith University, Australia
- "Challenges facing power BiCMOS integration," T. Efland, Texas Instruments, USA
- "Future microelectronics beyond roadmaps," S. Hillenius, Lucent Technologies Inc., USA
- "Quantum well intermixing for optoelectronic device integration," C. Jagadish, Australian National University, Australia
- "Diamond technology for MEMS and electronics: Review of status and perspectives," E. Kohn, University of Ulm, Germany
- "Semiconductor device for fiber optical communication systems," L. Lunardi, JDS Uniphase Corp., USA
- "Advances in silicon carbide power MOS technology," P. Mawby, University of Wales, U.K.

*Continued on next page*

## MIEL 2002 *continued*

- “Smart sensor interface electronics,” G. Meijer, Delft University of Technology, The Netherlands
- “Circuit design in multi-GHz environment,” V. Oklobdzija, University of California, USA
- “SiC device technology for high voltage and RF power applications,” M. Ostling, Royal Institute of Technology, Sweden
- “Integrated hall magnetic sensors,” R. Popovic, EPFL, Switzerland
- “Benefits of process and device calibration at early stages of CMOS development,” H. Puchner, LSI Logic Corp., USA
- “Trends in power ICs,” C.A.T. Salama, University of Toronto, Canada
- “Is innovation and competition crucial in the power semiconductor industry? A market perspective,” E. M. Shankar, De Montfort University Leicester, U.K.
- “Semiconductor technologies for powering microchips in the information age: From source to load,” K. Shenai, University of Illinois at Chicago, USA
- “Technology options for developing manufacturable nanoelectronics,” R. Singh, Clemson University, USA
- “MOCVD and PVD diffusion barriers for copper interconnect,” S. C. Sun, Taiwan Semiconductor Mfg. Co., Taiwan
- “Progress in intelligent power semiconductor devices,” Y. Uchida, Fuji Electric Co., Japan
- “Biologically inspired optical vision sensors,” J. Van der Spiegel, University of Pennsylvania, USA
- “Reliability of microsystems from the materials point of view,” J. Villain, University of Applied Sciences, Augsburg, Germany
- “Recent developments in silicon optoelectronic devices,” H. Wong, City University of Hong Kong
- “Silicon technology: Nanoscale CMOS and the road beyond,” P. Wong, IBM, USA

MIEL 2002 will be organized by the ED/SSC Yugoslavia Chapter, in cooperation with the Faculty of Electronic Engineering, University of Nis, and Ei-Holding Co.-Nis; under the cosponsorship of the IEEE EDS, with the cooperation of the IEEE SSCS; and under the auspices of Serbian Ministry of Science, Technology, and Development, Yugoslav Secretariat of Development and Science, Yugoslav Academy of Engineering, and City Assembly of Nis. ●

**Prof. Dr. Ninoslav Stojadinovic**  
*MIEL 2002 Conference Chairman*  
nino@unitop.elfak.ni.ac.yu

## AdCom Briefs

The Administrative Committee (AdCom) of the IEEE Solid-State Circuits Society met 4 February 2001 in San Francisco, before the start of the International Solid-State Circuits Conference. Ralph Wyndrum, IEEE Division 1 Director, provided the AdCom with an overview of the IEEE directions and challenges.

The AdCom made decisions on publications, conferences, and funding of a history project. It approved up to \$25K for the printing and mailing of a special issue of the *IEEE Transactions on Microwave Theory and Techniques* covering Integrated and Nonintegrated Silicon RF and Microwave Circuits. This special issue will be of interest to many SSCS members and so will be sent to them as well as to subscribers of the *Transactions on Microwave Theory and Techniques*. It is expected to be available in late 2001.

Bernhard Boser was approved as the new editor of the *JSSC* beginning in 2001. The AdCom approved the budgeting of 2140 pages for the *Journal* in 2002.



**SSCS AdCom. (l-r) Back row: Chris Mangelsdorf, Neil Weste, Stan Schuster, Bryan Ackland. Middle row: David Hodges, Richard Jaeger, Edgar Sanchez-Sinencio, Kiyoo Itoh, Gerhard Fettweis, John Corcoran, Bernhard Boser, Mark Horowitz, Anantha Chandrakasan, Kevin O'Connor. Front row: Anne O'Neill, Jonathan David, Christer Svensson, Gary Baldwin, Charles Sodini, Bruce Wooley, Lew Terman, Ralph Wyndrum, Asad Abidi, Jan Van der Spiegel.**

The Society will continue expanding its digital archives of key Society publications in solid-state circuits. The AdCom authorized an expenditure of up to \$130K to include the full archive of the *Digests of the Symposium on VLSI Circuits* in a merged *JSSC/ISSCC/VLSI Circuits* database and the printing of a DVD from it in 2002.

Anantha Chandrakasan was approved as Vice Chair of the ISSCC Program Committee. To support students' and others' travel to Society conferences, the AdCom approved up to \$20K to be available as matching funds to SSCS-sponsored conferences.

To help defray expenses for chapter chairs' travel to the Society



**The AdCom thanked John Trnka (right) for his outstanding service as Chairman of the Executive Committee of the International Solid-State Circuits Conference (1995–2001). SSSC President Bruce Wooley presented a plaque to Trnka in recognition and appreciation of his dedication.**

Chapter meeting held each February at the ISSCC, the AdCom approved up to \$10K.



**The SSSC Meetings Committee. (l-r) Stan Schuster, David Hodges, Mark Horowitz, Anantha Chandraksan, Rakesh Kumar. The AdCom approved two recommendations of the Meetings Committee: 1. Appoint Anantha Chandraksan as the Vice Chair of the ISSCC Program Committee 2. Establish matching funds to defray students' and others' travel expenses to Society-sponsored conferences.**

Up to \$15K has been approved for a Solid-State Circuits History Project. In conjunction with the IEEE History Center, the SSSC will record oral histories of prominent developers on a given topic within

the broad spectrum of solid-state circuits.

The AdCom will meet again 27 August in San Francisco to conduct Society business and to elect new officers for 2002. ●

## Expanded Eligibility for SSSC Candidates for President and Vice President

The SSSC AdCom recently voted to change the SSSC constitution to make it consistent with the bylaws regarding eligibility of candidates for president and vice president. Now both the constitution and bylaws state that candidates for president and vice president shall be past or sitting members of AdCom.

Prior this correction, the constitution had allowed that only “elected” AdCom members were eligible for election as president or vice president.

According to SSSC President Bruce Wooley, who proposed the change, “adopting the criterion specified in the bylaws opens up the nominating pool for vice president and president to qualified candidates who may have served the Society long and well as members of the AdCom and have invaluable experience with respect to the Society’s needs and operations. It also opens the candidacy to individuals with a demonstrated record of ser-

### EXISTING Section 6.1 (Nomination and Election of Officers) of the SSSC Bylaws:

In odd-numbered years, the Nominations Committee shall prepare a slate of candidates for President and Vice President. Candidates shall be present or past members of the Society AdCom, and shall have expressed a willingness to serve if elected.

### OLD Article V, Section 3 of the SSSC Constitution:

The Administrative Committee shall elect every two years a President and Vice-President. The President and Vice-President may not serve two consecutive terms, and must be past or sitting elected members of the Administrative Committee.

### REVISED Article V, Section 3 of the SSSC Constitution

The Administrative Committee shall elect every two years a President and Vice-President. The President and Vice-President may not serve two consecutive terms, and must be past or sitting members of the Administrative Committee.

vice and commitment to the Society who might not have the worldwide recognition often needed to win a closely contested AdCom election.”

Approval by the AdCom means the change is pending: the change will take effect 60 days after circulation to all the membership of this issue of SSSC Newsletter. The deci-

sion would only go to a full membership ballot if 5% of the members object to the change.

For your reference, you can find the full text of the SSSC Constitution and Bylaws at the SSSC website: [www.sscs.org/info](http://www.sscs.org/info). Select the button ABOUT to find the menu with links to the constitution and bylaws. ●

# SSCS EVENTS CALENDAR

Also posted on [www.sscs.org/meetings](http://www.sscs.org/meetings)

## SSCS Sponsored Meetings

### 2001 SSCTC Low Power Circuits Workshop

[www.ieee.org/ssctc](http://www.ieee.org/ssctc)

11–12 October 2001

Key Bridge Marriott, Arlington, VA

### 2002 ISSCC International Solid-State Circuits Conference

[www.isscc.org](http://www.isscc.org)

5–7 February 2002

San Francisco Marriott Hotel, San Francisco, CA

Paper deadline: 5 September 2001

Contact: Courtesy Associates, [ISSCC@courtesyassoc.com](mailto:ISSCC@courtesyassoc.com)

### 2002 CICC Custom Integrated Circuits Conference

[www.bis.com/~cicc](http://www.bis.com/~cicc)

12–15 May 2002

Caribe Royale Resort Suites, Orlando FL

Paper deadline: 28 November 2001

Contact: Ms. Melissa Widerkehr, [cicc@his.com](mailto:cicc@his.com)

### 2002 Symposium on VLSI Circuits

[www.vlssymposium.org](http://www.vlssymposium.org)

13–15 June 2002

Hilton Hawaiian Village, Honolulu, HI

Deadline for receipt of summaries: 8 January 2002

Contact: Phyllis Mahoney, [vlsi01@aol.com](mailto:vlsi01@aol.com)

or Business Center for Academic Societies Japan,

[vlsisymp@bcasj.or.jp](mailto:vlsisymp@bcasj.or.jp)

## Technically Cosponsored Meetings

### ISLPED 2001: International Symposium on Low Power Electronics and Design

[www.cse.psu.edu/~islped](http://www.cse.psu.edu/~islped)

6–7 August 2001

Huntington Beach, CA

Deadline: passed

Contact: [islped@cse.psu.edu](mailto:islped@cse.psu.edu)

### ESSCIRC 2001:

#### European Solid-State Circuits Conference

[www.eescirc.org](http://www.eescirc.org)

18–20 September 2001

Villach, Austria

Contact: Herbert Grünbacher, Carinthia Tech Institute, [hg@cti.ac.at](mailto:hg@cti.ac.at)

### BCTM: IEEE Bipolar/BiCMOS Circuits and Technology Meeting

[ectm.et.tudelft.nl/www/BCTM](http://ectm.et.tudelft.nl/www/BCTM)

Short Course: 30 September 2001

Conference: 1–2 October 2001

Minneapolis Marriott City Center

Minneapolis, MN

Contact: Janice Jopke, [jopke@aol.com](mailto:jopke@aol.com)

To maintain all your IEEE and SSCS subscriptions, email address corrections to:

**[address-change@ieee.org](mailto:address-change@ieee.org)**

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Piscataway, NJ 08855

