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SOLID-STATE CIRCUITS



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Solid-State Circuits Award to CMOS Circuit Pioneers

The 2000 Solid-State Circuits Award recipients, Robert W. Krambeck and Hung-Fai Stephen Law, are being honored for pioneering the introduction and implementation of domino CMOS logic. This form of dynamic logic requires only a single clock and offers the highest speed possible in CMOS logic, yet it is completely free from race conditions. It was the starting point for a new approach to CMOS logic, and its many variants are now indispensable in areas such as the design of high-performance microprocessors.

From the beginning of MOS tech-

nology, dynamic circuits have been used in DRAMs, shift registers, PLAs, and other highly regular digital arrays. Because of the potential savings in power, significant effort was devoted to the development of dynamic circuits for realizing general-purpose NMOS logic throughout the 1970s. This work typically resulted in complex multistage logic circuits. Moreover, race conditions in these circuits would result in errors unless multiple clocks were used to carefully propagate information from stage to stage. The need for multiple, carefully controlled clocks often led to disappointingly slow circuits.

In 1977, Krambeck, Law, and Charles M. Lee (deceased) conceived an elegant and definitive means of employing dynamic circuit techniques to reduce the area and improve the performance of digital circuits implemented in CMOS technology. Until the late 1970s, commercial microprocessors were realized with NMOS technology. CMOS emerged as an alternative to NMOS



Robert W. Krambeck

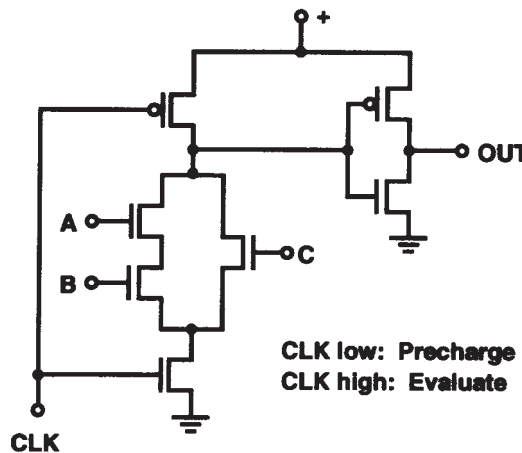


Hung-Fai Stephen Law

to conserve power without the complexity associated with dynamic NMOS circuitry. But CMOS gates were designed as static circuits, which were generally regarded as too large, and therefore too costly, for anything but niche markets. Krambeck et al. felt even then that CMOS was the wave of the future, but they realized that it would be necessary to eliminate as many of the redundant PMOS transistors as possible. Dynamic logic was the perfect means of accomplishing this, if it could be made reliable and simple enough. They then had the counterintuitive insight that the required simplicity could be obtained by adding a static CMOS inverter to the output of a precharged dynamic gate. The inverters were compact, low power, and could be used as buffers to drive large load capacitances, which in turn permitted the size of all logic transistors to be minimized. An even deeper insight was that all stages of logic would have inputs that were precharged to zero, so that only a single clock was needed. When the cascade of domino

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SSC Award to CMOS Circuit Pioneers *continued*

CMOS gates is clocked, no stage transitions until its predecessor has done so. Thus, information ripples down the cascade of gates at full speed, like a row of falling dominos.

Since domino CMOS gates are noninverting, they do not provide a universal set of logic elements. They are, however, by their nature input/output-compatible with static CMOS gates. Therefore, most logic functions can be implemented with domino CMOS either alone or in combination with a small amount of static CMOS logic. Krambeck, Law, and Lee first used domino CMOS in the design of an 8-bit arithmetic logic unit (ALU) and then in a subsequent 32-bit ALU. They discovered that the critical fast-carry path in these circuits could be implemented in domino CMOS together with a single static exclusive-OR gate at the output. This implementation proved to be twice as fast as a static CMOS realization and substantially more compact. The results of this work were published in 1981, and a patent was granted in 1983.

The work of Krambeck, Law, and Lee has proven to be the impetus for much subsequent work on high-performance digital CMOS logic design. Domino CMOS and its derivatives are now used in far more complex logic systems than were described in the original work, employing multiple static inverters and clocks as well as differential circuits in order to achieve the highest possible speed. These techniques are now widely exploited in high-speed VLSI circuits such as microprocessors and digital signal processors.

The recipients of the Solid-State Circuits Award solved an important and highly visible circuit problem that was becoming a major obstacle

“Charles Lee was a great help in reducing this idea to practice. When results were not what we expected, he was there with ideas on how to make it work,” said Robert Krambeck. “I am very sorry that he is not here to share in this honor.”

The untimely death of Charles Lee in December, 1989 makes him ineligible to share this award.

to the continued exponential growth in the scale of digital circuit integration. Their solution was a breakthrough in circuit design, and it has been widely praised and adopted by their colleagues.

Robert Krambeck is retired from Compaq Computers and cruising the North America's coasts west to east through the Panama Canal in his sailboat, “Best of Times.” He has no land-based residence at the moment. He began his professional career at Bell Laboratories after receiving a Ph.D. in Electrical Engineering from Carnegie Mellon University. As a Member of the Technical Staff at Bell Labs from 1968 to 1977, Krambeck did original work on trapping effects in silicon buried-channel devices as well as charge-coupled structures. From 1977 to 1982, as the Supervisor of Microprocessor Design, he managed the development of AT&T's 8- and 32-bit microprocessor families. From 1982 to 1989, he was responsible for the development of design methodologies for standard and custom ICs. The last 6 years of Krambeck's career at Bell Labs were spent as the Head of the Custom IC Design Department, where he was responsible for the development of FPGA silicon and software as well as integrated cir-

cuits for local area networks. From 1995 to 1998, Krambeck was the manager of Processor Development at Tandem Computers, where he supervised a 40-member staff developing fault-tolerant computers and the associated application-specific ICs.

After receiving a Ph.D. in Electrical Engineering from Columbia University, Steve Law joined Bell Laboratories. As a Member of the Technical Staff and then as a supervisor, he conceived and then developed the gate matrix approach to symbolic layout, coined domino CMOS logic, and contributed to the design of 32-bit CMOS microprocessors. As founder and R&D director at Cadence Design Systems from 1983 to 1990 Law, developed SKILL, a layout editor, layout automation tools, and logic synthesis tools. Between 1990 and 1994, he served in a variety of roles at Aptix Corp., including co-founder, vice president, COO, and director. There Law was responsible for the introduction and support of the new FPIC multichip system and later managed company operations. As a Vice President of Optivison, Inc. from 1995 to 1997, Law's responsibilities included the design, introduction, and support of a series of leading-edge MPEG video compression products. Presently, Steve Law is the Vice President of Alaris, Fremont, CA. At Alaris, Law is responsible for ASIC development, foundry arrangements, and Asian OEM sales. ●



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Vice President

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*The seminal paper relevant to this award is “High-speed compact circuits with CMOS,” in Journal of Solid-State Circuits, pp. 614–618, June 1982. This is a more complete version of a paper first presented at ESSCIRC in 1981. It is available now for \$22.95 through Ask *IEEE, the document delivery service of the IEEE. Fax: (303) 758-1138; Tel: (303) 759-2226; Within the U.S.: 1-(800) 949-4333; Email: askieee@ieee.org.*

Our thanks to the nominator

The Solid-State Circuits Society would like to express its thanks to Bernard T. Murphy for his nomination of Krambeck and Law, the recipients of IEEE Solid-State Circuits Award for 2000. Recognition of outstanding technical accomplishments and leadership is an important aspect of the IEEE and the Solid-State Circuits Society, and we greatly appreciate Dr. Murphy taking the time and effort to carry out the nomination.

Bernard T. Murphy received Ph.D. degree from Leeds University in 1959. In 1961 at Westinghouse, he invented the buried collector structure that since has been used in virtually all bipolar ICs. In 1963, he joined Bell Labs. In 1968, he (with V. J. Glinsky) coauthored an ISSCC Outstanding Paper involving

thinner epitaxial layers for new approaches to bipolar ICs. Later he managed R&D programs, including Twin-Tub CMOS, domino CMOS microprocessors; gated diode crosspoints for #5 ESS; and GaAs ICs for the first 1.7 Gb/s fiber optic system. In 1977 he was elected an IEEE Fellow and in 1982 received a Best Paper Award at ESSCIRC.

Bernie is retired from Bell Labs. He currently mixes scientific, musical, gardening, and construction activities in whatever blend seems appealing on a given day.

Bernard T. Murphy
Email: btjamurphy@aol.com



Nominees Sought for 2001 IEEE Technical Awards

The IEEE annually recognizes outstanding contributors worldwide to the art and science of electro- and information technologies with 22 technical awards. The SSCS Awards Committee supports the process by encouraging quality nominations and substantive endorsements from qualified peers. This January they will be wrapping up their work on nominations for 2001. The actual recipient selection is administered through the Technical Field Awards Council of the IEEE Awards Board.



The SSCS Awards committee encourages member suggestions for these awards nominations. Any person may nominate a candidate for an IEEE medal or award, but self-nomination is not allowed. Do you have possible nominees for the prestigious IEEE Technical Field Awards? Here are five of these institute-wide awards in the field of Solid-State Circuits that are especially important.

The Solid-State Circuits Award for outstanding contributions in the field of solid-state circuits to an individual or team of not more than three. Bronze medal, certificate, and \$10,000 cash prize are presented at the ISSCC.

The Clelio Brunetti Award for outstanding contributions in miniaturization in the electronic arts. Certificate and cash prize.

The Morris N. Liebmann Memorial Award for important contribution to emerging technologies recognized within recent years to an individual or team of not more than three. Certificate and cash prize.

The Frederik Philips Award for outstanding accomplishments in the management of R&D resulting in effective innovation to an individual or team of not more than three. Bronze medal, certificate, and cash prize.

The David Sarnoff Award for outstanding contribution in electronics. Preference given to an individual for achievement in the past 10 years; may be presented to a team of not more than three. Bronze medal, certificate and cash prize.

The nomination process consists of the nomination itself, letters from 3 to 5 endorsers, and a letter from the President or designee of the Society in the nominee's field. Instructions for the nominator, guidelines, and award criteria are available at www.ieee.org/awards/98guide.htm.

The nomination form can be filled in online or downloaded in a variety of word-processing formats from the URL: www.ieee.org/awards/noms/solidnom.htm.

Please send your recommendations no later than early January 2000 to:

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Fax: (334) 844-1888 ●

New SSCS Senior Members

Congratulations are extended to the following SSCS members for their recent promotion to IEEE Senior grade:

Allen, James D. Efendovich, Avner
Hagiwara, Yoshiaki Katopis, George

Kemp, C. J. Kirihata, Toshiaki
Kyung, Chong M. Lutz, Martin A.
Martin, Jean C. Quere, Raymond
Sridhar, R. Van Tran, Hiep
Zhu, Qing

The 1999 Custom Integrated Circuits Conference

This year's Custom Integrated Circuits Conference (CICC) was held in San Diego, CA from May 16 to 19 with close to 700 people registered for the conference. The focus of the conference was system-on-a-chip (SOC) design. A significant number of the technical tracks were focused on examples of SOC designs, design methodologies, and IP creation and management. New to the CICC was the IC design project management track. This track focused on the problems associated with the management of IC design projects and specifically of SOC designs. The overall conference program consisted, like the previous year, educational sessions, exhibits, exhibitor sessions, panel discussions, luncheon speakers, and the technical program.

Best Paper Award

This year, for the first time, CICC gave out an award for the best paper presented at the 1998 Custom Integrated Circuits Conference. The best paper award was given to Prof. Behzad Razavi of the University of California, Los Angeles, for his paper entitled, "CMOS technology characterization for analog and RF design." (This paper can be downloaded from the CICC Web site: www.ieee.org/conference/cicc)

Educational Sessions

Four parallel educational sessions were held. Each track had a particular focus, ranging from embedded memories and SOC to wired and

wireless communications. In the embedded memory arena, the different tutorial tracks took the attendees from process integration issues to the design and application of systems with [embedded] DRAM. The SOC topics covered wireless systems, testing, and software/hardware codevelopment. The wired and wireless communications track covered RF system design, front-end circuitry, PLLs, and frequency synthesizer design.

Keynote Presentation

The keynote speaker, Dr. Pallab Chatterjee, senior vice president of Texas Instruments, discussed the links between the Internet age and the SOC integration drive. The core of Dr. Chatterjee's presentation discussed the switch from Moore's law as the electronics industry main driver to Metcalf's law. Metcalf's law defines the communications and networking industry as the main driver, which brings us into the Internet age. Dr. Chatterjee focused on the different parts of the communications and networking landscape and how they impact the electronics industry: chip vendors, CAD tool vendors, service providers, entertainment, and others. A clear change that is recognized is the migration from a performance-driven to an integration- and cost-competitive-driven environment. Another important conclusion of the keynote speech is the role of packaging in future electronic systems. Dr. Chatterjee's presentation can also be downloaded

from the CICC Web site: www.ieee.org/conference/cicc.

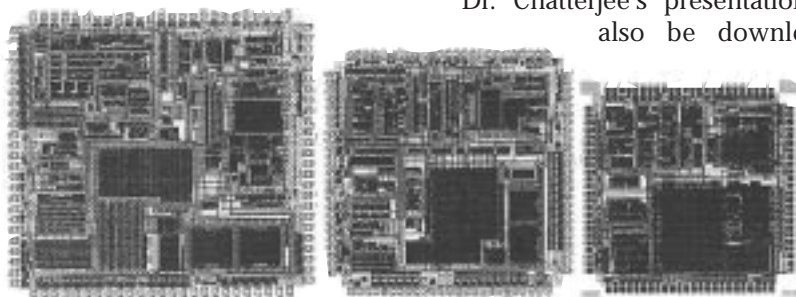
Luncheon Speaker

An interesting "intermezzo" in the conference was the conference luncheon presentation. This year's presentation was given by Dr. Peter Osman of the Cooperative Research Center for Molecular Engineering and Technology, Sydney, Australia. Dr. Osman's presentation, entitled "Soap, gold & athlete's foot: A guide to the construction of a biological field effect transistor," captured the audience with some real-world as well as future-world applications of the merging field of electronics and biology. The interested reader is referred to the Research Center's Web site: www.ambri.com.au/.

Technical Program

One of the most valued features of the CICC technical program was the invited papers. The majority of the sessions started with an invited paper that had either a tutorial or in-depth/exploratory character. These papers are double-length (e.g., the presentation lasts for at least 45 minutes), making them especially suitable for newcomers or for those that need a refresher on the particular topic. Out of a total of 137 technical papers presented, there were 17 invited and tutorial papers. It is impossible to cover in this retrospect every paper that was presented at the CICC. Instead, a few examples will be picked from the main categories that the CICC had defined for the 1999 conference. These main categories were system-on-a-chip (SOC) design and design methodologies, wired and wireless communications, analog design, embedded memory, test and reliability, digital signal processing, programmable devices, and process technology.

The CAD flow associated with SOC design was covered by an invited paper from IBM as well as a paper from CMOS Solutions, cov-



Read-channel ICs: The first (right) chip operates at 170 Mb/s, the last (left) chip operates at 400 Mb/s. Power dissipation has remained almost the same over these three generations.

ering issues related to the design of global signals in sub-0.25 μm CMOS designs. Additional papers covered new design methodologies in the area of high-performance clocking and power routing. Another significant CAD topic was the issue of noise. Several invited papers covering both the tutorial as well as the state-of-the-art angle provided an in-depth view of all the issues related to noise on a chip.

On the signal processing side, there was an excellent invited paper from Datapath Systems on the evolution of hard disk drive read channels and an invited paper from Lucent Technologies on the new generation of DSP architectures. The paper from Datapath Systems, entitled "Hard disk drive read channels: Technology and trends," gives an excellent overview of the advances that have been made in IC design in general and in a whole set of sub-fields, ranging from magneto-resistive heads, magnetic storage materials, analog and digital signal pro-

cessing, to CAD tools geared toward analog design. The figure on page 4 shows three very recent generations (within a 2-year spread) of read-channel ICs that had significant commercial market share.

In the area of wireless systems, the 1998 Best Paper Award winner Behzad Razavi presented an invited paper on "RF Transmitter Architectures and Circuits." In addition, there were several sessions devoted to the different building blocks that are required to build wireless SOCs (e.g., papers from Philips, IBM, Philips Electronics). Papers from Berkeley, Cadence, Motorola, and Lucent also properly addressed the CAD aspects of wireless system design.

The process technology developments were covered by an invited paper from IBM that discussed device and circuit design issues in SOI technology as well as an invited tutorial paper from the University of Frankfurt, Germany that discussed the use of SiGe HBT technology modules for wireless communication ICs.

IEEE Journals to have Special Issues on CICC 99

Two journals will devote a special issue to the 1999 CICC: the *Journal of Solid State Circuits* and the *Journal of CAD*. Please refer to CICC's Web site: www.ieee.org/conference/cicc for more information as well as the best paper and keynote presentations, which can be downloaded.

Final thanks go to the people that made CICC 99 possible: the authors, presenters, members of the Technical Program Committee (TPC) and their respective companies, the IEEE, CICC exhibitors and sponsors, and Widerkehr and Associates.

We hope to see you at CICC 2000, May 21-24, in Orlando, FL. ●



Mike Beunder
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CICC 2000 Call for Papers Deadline December 1, 1999

Approximately 140 papers addressing a broad range of leading-edge circuits, applications, design techniques, and tools will be presented in Orlando, FL, May 21-24 at CICC 2000, including the latest in mixed-signal ASICs, embedded memories, and 0.18 μm technology.



Prospective authors must submit CAMERA-READY papers, up to four pages in length, inclusive of all illustrations, charts, and tables. Those interested in submitting papers should contact the Conference Office as early as possible to obtain an author's kit and detailed instructions. The address is: CICC, 101 Lakeforest Blvd., Suite 400B, Gaithersburg, MD 20877, Tel: (301) 527-0900 (ext. 316), fax: (301) 527-0994, email: cicc@his.com, URL: www.ieee.org/conference/cicc.

ACCEPTED PAPERS WILL BE PRINTED IN THE PROCEEDINGS WITHOUT OPPORTUNITY FOR FURTHER CHANGE. Papers should report original and previously unpublished work, including specific results. Circuit-oriented work must include measured experimental results. Appropriate company and government clearances MUST be obtained prior to submission. Authors of accepted papers will be notified by mail by January 27, 2000.

Call for Fellow Nominations Deadline March 15, 2000

The grade of Fellow is one of exceptional distinction, conferred by the IEEE Board of Directors on members who have significantly contributed to their technical field. The number of SSCS members nominated for Fellow this past year was well below that for other IEEE societies of comparable size. As a society, we simply are not doing an adequate job of recognizing the very significant contributions our members have made to our profession.

The Fellow nomination process is relatively straightforward but requires some forethought and planning preceding the March 15, 2000 deadline. Both a nominator and five references from current Fellows are required. If the nominee has not applied for senior member status, that application and its three supporting references must be submitted no later than February 4, 2000. Senior member forms can be emailed or completed online.

Email: Senior-member-forms@ieee.org
URL: www.ieee.org/organizations/rab/md/smforms.htm
Fellow kits can be requested in hard copy format or downloaded from the Web.

Fax: (732) 981-9019 Email: fellow-kit@ieee.org
URL: www.ieee.org/about/awards/table1.htm

1999 Symposium on VLSI Circuits Summary

The 1999 VLSI Circuits Symposium was held in Kyoto, Japan in conjunction with the VLSI Technology Symposium. This close association provided opportunities for people in technology and circuits and system design from many nations to interact. A highlight of both symposia was the Joint Rump Session, this year entitled "SOI: What are the road blocks, if any, to becoming a mainstream technology?" Panelists from a number of disciplines, including design, process, and wafer production discussed the tradeoffs from a number of points of view. The discussion became quite lively, with many members of the audience exchanging views with the panelists on such issues as manufacturing and circuit performance. The panelists and the audience divided into two distinct camps, depending on their view of the future of SOI. A detailed account of the animated exchange has been covered in several trade magazines.

The VLSI Circuit Symposium covered all aspects of transistor-level design, including imagers, pattern recognition, memories, microprocessors, and analog and high-speed serial links. This year, 393 people from 18 countries attended the symposium. There were 52 papers presented, chosen from 146 papers that had been submitted from 16 countries. In addition, four invited papers were presented.

The day prior to the symposium, T. Enomoto and Y. Sugimoto of Chuo University organized a 1-day short course, "System LSI and the related design technology." The course started with a discussion on a "Single chip MPEG2 encoder" by E. Ogura of Sony U.S. Research Laboratories. This was followed by a class, "Processor design for multimedia processing" by T. Arai of NEC. T. Watanabe of Hitachi finished the morning by describing an embedded DRAM architecture. In the afternoon, K. Ueda of Matsushita dis-

cussed "Digital signal processors for mobile terminals." The course then shifted to implementation topics, as T. Kuroda of Toshiba discussed "Low-power CMOS digital design" and Steve Butler (AMD) and Dan Bailey (Compaq) discussed "High-performance clocking," which, with each generation becomes an increasingly difficult design problem. Finally, K. Soumyanath of Intel discussed "Interconnect design for system LSI."

Each of the first 2 days of the symposium started with invited talks. F. C. Tseng of Taiwan Semiconductor Manufacturing Company discussed "Semiconductor industry evolution for the 21st century." He concluded that the semiconductor industry is entering a new era in which the norm is vertical disintegration. Bijan Davari of IBM presented his invited paper entitled "CMOS technology: Present and future." Dr. Davari showed the audience that innovations such as copper interconnect and SOI are required to maintain historically established performance trends.

The symposium has had a tradition of reporting significant breakthroughs in the memory area, and this year was no exception. Paper 13-2, "A 7F2 cell and bitline architecture featuring tilted array devices and penalty-free vertical BL twists for 4 Gb DRAMs" was presented by H. Hoenigschmid.

This joint effort involving IBM and Siemens featured a 30-degree tilted array device and a clever scheme to twist the bitlines while avoiding a break in the array. Paper 4-4, "A 144Mb 8-level NAND flash memory with optimized pulse width program-



Dr. Davari (IBM) argues that copper interconnect and SOI are required to maintain historically established performance trends.

ming" by Hiromi Nobukata et al. featured high-programming throughput by controlling both the bitline voltage and the programming time depending on the programming data.

Another very popular theme this year was high-speed serial links. A wide variety of state-of-the-art approaches was presented. Raman Fajad-Rad et al., in Paper 5-1, "A 0.3 μm CMOS 8-Gb/s 4-PAM

serial link transceiver," achieved their frequency serial link by multiplexing and demultiplexing the data directly at the I/O pad to avoid high on-chip frequencies. Another high-speed interface, which was designed as a component of an ASIC standard cell, was reported by Ah-Lyan Yee et al. in Paper 5-2, "An integrable 1-2.5Gbp/s low jitter CMOS transceiver with built-in self-test capability."

In the analog area, high performance was also a pervasive theme. Paper 8-1, "A 10b, 400 MS/s glitch-free CMOS D/A converter," was authorized by K. Khanoyan et al. Continuing this theme, Paper 8-2 by Koichi Irie et al., "An 8b 500 MS/s full Nyquist cascade A/D converter," explained the use of a 27-GHz bipolar process. Additionally, Hirad Samavati et al. presented Paper 9-2, "A 12.4 mW CMOS front-end for a 5GHz wireless-LAN receiver." This circuit featured a high-speed differential circuit with inductive elements.

Sensors and imagers played a big role in the 1999 VLSI Symposium. T. Lule et al. offered Paper 14-1, "A 100,000-pixel 120 dB imager in TFA-technology," which explained an imager fabricated using a thin film on ASIC technology. In addi-

The Proceedings of the 1999 Symposium on VLSI Circuits [IEEE Cat. No. 99 CH36326] contain all the papers presented but not the details of the short course presentations. For soft- or hardbound copy or CD-ROM, order through IEEE Customer Service (800) 678-4333 or (732) 981-0060 (outside the U.S. and Canada), fax (303) 758-1138, email: askieee@ieee.org.

tion, Paper 16-1, "A high-resolution capacitive fingerprint sensing scheme with charge-transfer technique and automatic contrast emphasis," by Hiroki Morimura et al. and Paper 16-2, "CMOS fingerprint sensor with automatic local contrast adjustment and pixel-paral-

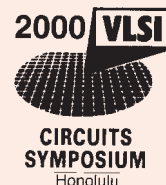
lel encoding logic," by Stefan Jung et al., both dealt with the algorithms and circuits for the encoding of fingerprint images. These imaging papers represent true system-on-a-chip implementations.

We hope you can join us next year, June 15-17, 2000, when the

symposium will convene in Honolulu, Hawaii, so that you may experience all aspects of the VLSI Symposium.

• **David Scott**
Technical Program Cochair
david.scott@ti.com

2000 Symposium on VLSI Circuits Call for Papers Deadline January 2, 2000



The emphasis will be on circuit design. Papers will be considered on the basis of originality and quality. Although the circuits need not necessarily be implemented in a semiconductor chip, measured results, particularly for analog submissions, are desirable. There will be several invited papers on emerging VLSI circuit technologies.

To assure compliance with submission details, download the complete Authors' Guide, Paper Preparation Kit, copyright form, and instructions for the 75-word-abstract instructions from the Symposia's Web site: www.bcasj.or.jp/vlsi_sym/.

Submissions from universities are encouraged. Partial travel expense support for students who are presenting papers is available on request.

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IEEE Y2K Standards Online

As a public service, the IEEE Standards Association is providing access to two newly approved IEEE Computer Society Y2K standards at no charge. IEEE standards are normally available only on a fee basis.

[IEEE Standard for Information Technology—Year 2000 Terminology \(IEEE Std 2000.1-1999\)](#) defines terms and concepts for addressing Y2K issues for information technology. The standard revises a previous release and includes changes in requirements for claims of conformance. The new standard specifies that components and systems perform correct date processing for a minimum of 10 years, including 1999 and 2000.

[IEEE Recommended Practice for Information Technology—Year 2000 Test Methods \(IEEE Std 2000.2-1999\)](#) is an extensive compilation of recommended testing methods.

These standards are on the Web in PDF format at grouper.ieee.org/groups/2000/index.html.

ISSCC Short Course to be Developed on CD-ROM

The Educational Activities Committee of the SSCS is currently in the evaluation stage of a program to produce one or more of the short courses of the ISSCC in an interactive CD-ROM format. The committee has produced a demo CD based on selected material, professionally compiled from the 1999 ISSCC short course program. Following an evaluation by the committee and members of the AdCom and the ISSCC ExCom, it is agreed to produce a complete short course program in the near future. It is our belief that the timely value of these courses can be enhanced through broader availability. The universal access to high-quality multimedia CD-based PCs makes an interactive CD ideal for SSCS members and IEEE members-at-large. We will keep you posted on the progress of this effort through this newsletter.



Kevin O'Connor
Education Activities Chair
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Chapters Round-Up

The SSCS has grown from one chapter in May of 1997 to its current status of 20 chapters. Half of our chapters are now in Region 8 with three new chapters in Russia, two in Novosibirsk (one "regular" chapter and one student chapter at the Novosibirsk State Technical University), and one in Novgorod. The addition of the Atlanta and Montreal chapters has also expanded SSCS membership in North America. The Sharif University of Technology in Iran is another new student branch chapter. We hope the news of technical meetings and activities in Latin America is the first hint of chapter formation in Region 9.

In other chapter news, 1999 also marked the first year of the SSCS chapter subsidy program. Many of the events and activities that are mentioned in the following articles are a direct result of the successful subsidy program implemented by the SSCS. The popularity and success of the subsidy program is demonstrated in many ways. All of the eight chapters (Baltimore, Boston, Taipei, Tokyo, Chicago, Yugoslavia, Seoul, and Finland/Estonia) that received subsidies for 1999 reapplied for subsidies in 2000. The number of chapters applying for the SSCS subsidy has increased from 8 to 14.

The following are summaries of some of the activities in which various SSCS chapters were involved.

Estonia

Chair: Vello Kukk

From February to May of this year, the Estonia chapter held nine meetings, featuring speakers from industry and academia. One student presentation by Raido Kurel on nanotechnologies was also scheduled. The chapter awarded two gift memberships for best students this year and supported the publication of the Proceedings of the 6th International Telecommunications Conference that included eight student papers. In the fall of this year, the Estonian chapter is planning activities with nearby

Baltic countries: an Estonian-Swedish Workshop on "Mixed analog-digital IC design" and a Finland section meeting on September 30 in Tallinn, Estonia are scheduled.

Ireland Chapter

Chair: Peter Kennedy

Ireland Chapter Kicks Off

Jan Rabaey of UC Berkeley was the speaker at the Inaugural Lecture of the SSCS Ireland chapter at Trinity College, Dublin in June. Before an audience of 40 circuit designers from Ireland's growing ASIC design community, Rabaey addressed issues on "Ultra low power software definable radio design using reconfigurable processors." He discussed new trends in radio technology, particularly those toward better spectrum utilization through the use of aggressive DSP solutions and design partitioning for software radio.

The underlying theme of the talk was the need for hardware that adapts to the application. Rabaey asserted that if this is to be achieved, then specific metrics such as energy per stage, delay per stage, and energy delay product per stage must be applied to assess the design at all stages of its development.



IEEE Board of Governors delegation views Virtex chip at Xilinx, as part of their 2-day tour of Ireland. l-r: Brendan Cremen (R&D Director, Xilinx Ireland), James Christie (Irish Representative, IEE UKRI Section), Peter Kennedy (University College, Dublin), Cecilia Jankowski (IEEE Staff Managing Director-Regional Activities), Don Loughry (IEEE VP-Standards Activities), Arthur Winston (IEEE VP-Educational Activities), and Dan Benigni (IEEE VP-Regional Activities).

The talk was cosponsored by Analog Devices, Massana, Silicon and Software Systems, Silicon Systems Limited, and Xilinx Ireland.

IEEE Board of Governors Delegation Visits Ireland

Following the June IEEE Board of Governors Executive Committee meeting in London, a delegation visited Ireland on June 9 and 10. The first port of call was the National Microelectronics Research Center in Cork, the inspiration for much of Ireland's thriving electronics industry.

"Challenges facing the electrical and electronics industry in Ireland: What we're doing right and what we should change" was the topic addressed by delegates representing industry, academia, and national development agencies at the Open Discussion Forum in Dublin the following day. Lively debate was followed by stimulating site visits to two multinational electronics companies, one Dutch and one American, and two Irish startups, Silicon Systems Limited and Massana, which are rapidly growing their silicon IP portfolios.

Novosibirsk, Russia

Chair: Boris Y. Kapilevich

The Novosibirsk chapter has existed for a number of years as a joint chapter of four related technical societies: Electron Devices; Microwave Theory and Techniques; Communications; and Components, Packaging, and Manufacturing Technology. This spring, the chapter added SSCS to their joint technical focus. They began immediately organizing a student seminar, "Designing solid-state circuits for wireless applications," held at Siberia State University of Telecommunications in June 1999. Currently, the chapter is active in the organizing a session on

“Solid-state circuits components and devices” at the International Conference on Actual Problems of Electronics Instrumentation Engineering (APEIE-2000), Novosibirsk, Russia, scheduled for September 2000.

Novosibirsk Student Chapter

Chair: Vladimir V. Galushkin

The new SSCS student branch at Novosibirsk State Technical University has begun to set up a chapter Web site. They also plan to establish an IEEE Student Branch Center of Excellence. This will include an Open Student Design Laboratory and associated Web site. As the year progresses, the chapter will be organizing technical support for the 1st Siberian IEEE-Russia Student Workshop on Electron Devices and Materials. This workshop is scheduled as part of the 5th International Conference on Actual Problems of Electronics Instrument Engineering (APEIE-2000), Novosibirsk, Russia. The chapter's faculty advisor is Alexander V. Gridchin.

Sharif University, Iran Student Chapter

Interim Chair: Alireza Motieifar

Even before this new SSCS chapter was officially recognized, the 14 student members at Sharif University of Technology held three meetings. Dr. B. Rashidian presented an interesting lecture on “Electronics today” for the first meeting. At the second meeting, Dr. M. S. Baghini reviewed the current methods for analog circuit design automation and proposed a novel approach for automatic design of analog circuits based on circuit behavior. At the third meeting, Dr. A. Fotowat talked about high-speed data transmission techniques and circuits.

On September 20 and 21, the student chapter scheduled a 2-day workshop on photonics. Dr. H. Kaatuzian, Dr. B. Rashidian, and Dr. J. Sadeghi will present lectures in the following subjects: MOEMS, photo detectors, optical fibers, non-linear optics, and optical integrated circuits.

The students at Sharif University of Technology are proud of their famous graduates, B. Razavi, F. Behbahani, and A. Hajimiri. They are planning weekly meetings with their advisor, Dr. Ali Fotowat, a specialist in RF CMOS IC design.

Seoul, Korea

Chair: Moon K. Lee



This joint chapter with EDS heard presentations from three IEEE Distinguished Lecturers in 1999.

Prof. Thomas H. Lee of Stanford University and

IEEE SSCS Distinguished Lecturer presented his technical talk on CMOS RF ICs, emphasizing the current status of the CMOS RF IC design technologies and design examples, such as a single-chip 1.6 GHz GPS receiver, a 5 GHz LNA/mixer/synthesizer, and 1.8 GHz VCOs. This seminar, held at Yonsei University in June, was attended by 150 from both academia and industry.

In March, Prof. Woodward Yang of Harvard University spoke on merged memory logic to 60 attendees at IDEC (Integrated Design Education Center) of Hanyang University: <http://idec.hanyang.ac.kr>.

Dr. Hiroshi Iwai of Toshiba, Japan was invited to present the plenary paper, “Downsizing of CMOS toward deep sub-0.1 μm limitation” at the 6th Korean Conference on Semiconductors (KCS),



IEEE SSCS Distinguished Lecturer Prof. Thomas H. Lee of Stanford University spoke on CMOS RF ICs at this seminar at Yonsei University.

Feb. 9–11, 1999. This technical talk was sponsored by both the IEEE ED Korea chapter and Seoul chapter. At the conference, 839 participants registered, 354 papers (223 oral and 124 posters) were presented, including invited papers, and there were 33 exhibit booths. After this meeting, the IEEE ED Korea chapter and Seoul chapter had a joint dinner meeting with Dr. Iwai.

The Seoul chapter sponsored the local IEEEK CAD and VLSI conference on May 8, 1999, at Sungkyunkwan University, Suwon, Korea. Sixty-four papers were presented during this conference. Six distinguished papers out of 20 written in English were selected, and each author was awarded a certificate and prize in the name of IEEE Seoul chapter.

A major effort of the chapter this year was the inaugural Asian-Pacific-ASIC conference held Aug. 22–24, 1999, at Yonsei University, Seoul, Korea. At the time of publication of this newsletter, 110 technical papers had been submitted from eight countries. This conference was sponsored by the IEEE SSCS, the IEEE SSCS Taipei chapter, and the IEEE SSCS Tokyo chapter.

SSCS Taipei Chapter

Chair: CK Wang

Since its official formation in July 1998, the SSCS Taipei chapter has sponsored and/or organized many events and activities. All of the activities sponsored by the SSCS TPEC (Taipei chapter) drew a huge audience, and many were even overbooked. As a result of this very positive reception, SSCS TPEC has become well known in industry as well as in academia.

Good speakers with pertinent topics are one of the major reasons for the success of the chapter's activities. One of these speakers was Prof. Paul Gray of the University of California, Berkeley. Prof. Gray spoke about “Recent development in integrated CMOS RF transceiver for personal communications.” Prof.

Continued on next page →

Chapters Round-Up *continued*

Gray was one of three speakers in the series "CMOS wireless transceiver circuit designs." The series, held June 14 at the National Chao-Tung University, Hsinchu, was attended by 244 people. In addition to lecturing, Prof. Gray promoted the SSCS and encouraged students and engineers to apply for membership.

In addition to these factors, good coordination and organization by the staff of the Chip Implementation Center (CIC) as well as participation from research institutions and VLSI industries promoted chapter growth and progress. Financially, the chapter received generous donations from sources such as the Ministry of Education (MOE), National Science Council (NSC), Industrial Technology Research Institute (ITRI), and various VLSI companies.

Another important event for the Taipei chapter was a visit in June by the President of the SSCS, Dr. Lew Terman. While he was there, Dr. Terman updated the chapter about what SSCS headquarters had done as well as its plans. Dr. Terman showed a genuine concern for the progress and needs of the Taipei chapter.

As far as the future is concerned, the Taipei chapter has many plans for the year 2000. It plans to organize a few seminars and cosponsor various circuit design activities with the NSC and MOE Advisory office. Another dimension that the chapter would like to focus on is holding student membership drives at major universities.

Tokyo Chapter

Chair: Hajime Ishikawa

For 2000, the Tokyo chapter will continue its popular tradition of holding meetings specifically for young engineers, which review key papers presented the preceding month at SSCS conferences, the ISSCC, and the CICC. During the year, the chapter cosponsors 10 two-day technical meetings with the Institute of Electronics, Information, and Communications Engineers (IEICE). Additionally, they will cosponsor with the IEICE a System

LSI Workshop at Biwako Lake in November 2000. In September, they sponsored a tutorial seminar on LSI design for beginners at the VLSI Design Education Center in Tokyo (VDEC). One of the two meetings scheduled with a Distinguished Lecturer next year is planned to assist in the establishment of a new chapter in west Japan at Kyoto, Kansai.

Yugoslavia Chapter

Chair: Ninoslav Stojadinovic

In March of this year, the Yugoslavia section organized a promotional campaign to attract undergraduate students to join the IEEE. An IEEE Electron Devices Society student chapter was formed. There are plans to enlarge the scope of the student chapter to include SSCS next year.

The organization of an International Conference on Microelectronics (MIEL'99) is the main activity of the joint chapter. This year, for the first time, MIEL received cosponsorship support from the IEEE Electron Devices Society, the other society that is the focus of the Yugoslav joint chapter in addition to Solid-State Circuits. The September conference was postponed because many authors from western countries were unable to get permission to travel to Yugoslavia during the crisis. Despite the war, the chapter has continued with the organization of this event. Instead of in September 1999, it will be held in May 2000 (the exact date is still to be decided). Two workshops with five invited lectures each are scheduled in conjunction with the conference on "Power devices and ICs" and "Microsystem technologies." The MIEL Proceedings went to press in August 1999. The Proceedings contain 18 invited and 136 contributed papers (74 oral and 62 poster) by authors from 34 countries. A short course, "Low-power electronics" by Krishna Shenai (University of Illinois at Chicago), will also be offered at the conference.

Professor Shenai, an IEEE EDS Distinguished Lecturer previously

presented a successful 5-hour tutorial on "Ultra-low-power RF micro-systems" at the University of Nis in December 1998. He visited EI Holding Co., Nis, the largest manufacturer of electronic products in Yugoslavia. Later, at the IHTM Institute, Belgrade, Professor Shenai held an outstanding lecture on "RF microsystems and power electronics for the next millennium." The chapter looks forward to the return to normal mail delivery of technical journals.

Zurich Chapter

Chair: Qiuting Huang

The inaugural meeting of the new SSCS Zurich chapter took place March 25, 1999 at ETH (Eidgenössische Technische Hochschule) Zurich. Approximately 30 members from both universities and industry around the country were in attendance. The industrial representation covered companies such as Philips, Siemens, EM Microelectronics, HMT, and others. Professor Qiuting Huang of the Swiss Federal Institute of Technology (ETH), Zurich was elected chair of the chapter.

The chapter meeting was followed by a colloquium on mixed signal integrated circuits. Six speakers from two ETH institutes covered topics such as microsystems for short-distance ranging, analog decoding for communications, and RF IC design.

Christoph Kuratli showed a novel method for short distance measurement, demonstrating how such a system can be implemented as a fully integrated solution. He also explained package-related limitations to accuracy.

M. Helfenstein presented a paper on decoding in analog VLSI. Because the iterative decoding of state-of-the-art error-correcting codes such as turbo codes is computationally demanding, he argued that analog implementation of such decoders can be much more efficient than digital implementation can be. An analog computing network for decoding turbo codes was shown to outperform digital decoders by two orders

of magnitude in terms of speed and/or power consumption.

The rest of the colloquium was devoted to RF circuits, including talks on a power amplifier (Ch. Yoo), a 1-GHz CMOS VCO/prescaler set for very-low-power applications (D. Pfaff), a 200-MHz, sub-mA BiCMOS RF front-end IC (A. Deiss), and a CMOS GSM transceiver IC (P. Orsatti).

The next colloquium is planned for this autumn at ETH Zurich.

Chicago Chapter

*Reports submitted by
Michael A. Banak,
Secretary*

"Internet telephony"

*Chuck Byers,
Distinguished Member of
Technical Staff
Lucent Technologies, Bell Labs*

The Chicago joint chapter of the IEEE Solid State Circuits, Circuits and Systems, and Electron Devices Societies held its winter meeting at the Motorola Center in Schaumburg, IL, Wednesday, January 13, 1999. Twenty-four IEEE members plus 11 guests heard Chuck Byers, Distinguished Member of Technical Staff with Lucent Technologies, give a lively 2-hour talk on "Internet telephony."

Being a member of Bell Labs' Advanced Architecture Team has placed Byers in a unique position to give us an accurate view of this emerging technology.

Among points of particular note is the existence of Internet Time, somewhat analogous to "Dog-Time," where events happen very fast but a "lifetime" for a product or technology could be a mere 3-4 years. In fact, Byers indicated that the information he shared would likely be obsolete within a year.

In defining Internet telephony, Byers explained that this technology carries packetized voice as either IP packets or ATM cells on high-speed facilities and fast switches and routers. Because this voice data shares bandwidth with other data in the network, it seems natural to transport other applica-

tion-specific data with the voice traffic, thus enhancing the possible uses. The key is to push the point of analog/digital conversion right up to the customer's premises, so that voice and digital services can be merged at that point and enable a whole new world of applications.

Today's simplest application in Internet-based telephony involves the use of current modem access. The sound quality, being transported through a mere 56 K modem, is poor, but the voice/Internet bridge has been made. Even with this crude, existing structure, it is possible to sustain a 24-hour voice connection to a relative overseas, while having to pay only local telephone access charges and a flat-rate Internet access fee. Except for the local access, this scheme, of course, bypasses the Public Switched Telephone Network and thus is a major threat to the incomes of those who manage this network.

In an advanced IP-based local access model, almost everyone has broadband digital access, through a cable modem, ADSL, or a corporate LAN or WAN. The voice A/D conversion occurs at the POTS station at a customer's premises and is immediately merged with other digital services, such as video conferencing, education, library access, database access, etc. It is generally agreed that future network access will be rich with graphical content, perhaps HTML based, thus making the merger with desktop PCs all the more natural.

Even though long-standing manufacturers such as Lucent and Nortel have a stake in providing equipment for the existing telephone network, they are working feverishly to match the activity of new firms like Cisco and Ascend, who make equipment geared for Internet access and bridging.

The scope of Chuck Byers' discussion was a pleasant surprise and somewhat of a wake-up call to many of the attendees. Also, he generously expressed a willingness to provide an updated version of the

talk a year from now. The importance and timeliness of this subject makes his suggestion a strong possibility for next year's schedule.

"Ultra low-power rf microsystems for the next millennium"

*Krishna Shenai, Ph.D.,
Prof. Electrical Engineering,
University of Illinois,
Chicago Circle Campus*

The Chicago joint chapter of the IEEE Solid State Circuits, Circuits and Systems, and Electron Devices Societies held its spring meeting at Lucent Technologies, Naperville, IL, on Tuesday, March 30, 1999. Eighteen IEEE members plus six guests heard Dr. Krishna Shenai, Professor of Electrical Engineering, University of Illinois, Chicago, give an impressive 90-minute talk on "Ultra low-power RF microsystems for the next millennium."

Dr. Shenai manages two research labs at UIC, the Power Electronics Research Lab (PERL) and the System on Silicon Research Center (SYSREC).

Opening with a broad overview of the general subject of systems-on-a-chip, Dr. Shenai showed how his labs and those around the world are integrating analog, digital, power systems and micromachine electrical-mechanical systems (MEMS) on one chip.

One surprising assertion in the talk was the deduction that CMOS would remain the technology of choice while going deep into system-on-a-chip development. Although CMOS may not surpass other technologies in areas like noise figure or bandwidth, its performance is still quite adequate for most tasks. Thus, its exceptionally low cost will make it the focus of further research for some time to come.

Presentation of the camera-on-a-chip concept was very well received. Using a CMOS active pixel technology, it is possible to integrate optical detection and signal processing for interface with

Continued on next page →

Chapters Round-Up *continued*

PCs for everything from robotic control to video teleconferencing.

One vision of the ultimate RF system would include the RF front end, the power amplifier, and all of the subsystems from these points to the user, all on one IC. At the RF front end, the high-frequency input would be quickly down-converted, where it would be A/D-converted and demodulated with digital signal processing techniques. This would bypass the power-hungry and less-accurate analog circuitry usually associated with these functions. In the best case, there would not even be a down-conversion but rather an immediate, very-high-speed analog-to-digital conver-

sion and then hand off to a DSP for demodulation. One of the critical issues here is to avoid input overload.

Integration of high-Q magnetic components continues to be a problem. But with emerging micro-machined techniques, it is possible to fabricate such magnetics so that they are suspended well above that lossy substrate, perhaps by creating a hollow area just below the integrated inductor.

This, in turn, allows for, among other things, fully integrated switching regulator power conversion systems. At sufficiently high switching frequencies, the size of the magnetics lends itself to possible integration.

Even though many problems remain to be solved for the most-complex systems, a feeling emerged from the talk that the vision of full mixed-signal system integration, even for electro-mechanical systems, was now within the realm of reality within the next generation, and that those not working on it are missing out. ●



Thanks to Janak Bhimani, SSCS summer intern, who compiled chapter reports and subsidy requests.

Integrated Circuits and Systems Events in Latin America (IEEE Region 9)

During 1999 in Latin America, the following events brought together specialists and students in the area of solid-state circuits.

Iberchip'99: Lima, Peru, in March

During Iberchip'99, 90 attendees from Region 9, Spain and Portugal, attended a week-long course on analog integrated circuits design. Originally organized 3 years ago by Prof. Paul Jespers (Belgium), IEEE SSCS Chapters Committee member and long-time collaborator of the SSCS, the course has become an annual event in Region 9. Held in Puebla, Mexico in 1997, and in Mar del Plata, Argentina in 1998, this course initially drew 40 students and engineering faculty attendees each year. The course's reputation has grown so that this year the level of participation has doubled. This year, IEEE SSCS Distinguished Lecturers Eric Vittoz and Willy Sansen taught the course in Lima. Iberchip has been organized and funded by the European Union International Cooperation Program.

14th International Congress on Microelectronics (ICMP99): Campinas, Brazil, August 3-6

The Brazilian Microelectronics

Society (SBMICRO) organized its Congress on Microelectronics (ICMP99), which included 8 tutorial lectures, 46 full papers, and 17 poster presentations. The technical sessions dealt with IC design, device, and process technologies. At the opening session, SSCS Secretary and Distinguished Lecturer Asad Abidi delivered the featured invited lecture. The full program of ICMP99, cosponsored by the International Microelectronics IMAPS organization, is available at davinci.lpm2.fee.unicamp.br/icmp99.

13th International Symposium on Circuits and Systems Design: Natal, Brazil, Sept. 29-Oct. 2

This event has been jointly organized by the Brazilian Computer Society and Microelectronics Society (SBCCI) since 1983 and brings together in Latin America the best technical work in the fields of IC and systems design and CAD methodologies for IC design. A total of 40 papers were presented at the 1999 program, outlined and available at www.dimap.ufrn.br/~sbcci99. The proceedings of this symposium have been published since 1997 by IEEE Computer Society Press.

In the year 2000, the SBCCI 2000

and SBMICRO conferences will be held in Manaus, Brazil.

New member and new chapter opportunities

A special new membership offer was extended to Latin American attendees to Iberchip, SBMICRO1999, and SBCCI1999 Symposium of Integrated Circuits and Systems Design. The offer of free Society membership and \$25 off IEEE membership was available through discount vouchers like those offered in past years at the ISSCC. Also there was information available on how to organize an SSCS chapter in the attendee's geographical area. Committed to helping the solid-state circuits technical community, the IEEE SSCS will support chapter activities that are organized by at least 12 members of the Society. ●



Sergio Bampi
AdCom Region 9
Representative

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Circuits Society
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TAB VP-Elect Candidate Statements

The election of the Technical Activities Vice President - Elect, will be on the fall IEEE ballot. Candidates are Roger B. Pollard, Chair

TAB Electronic Products Committee and Lewis Terman, President Solid-State Circuits Society. The candidates' position statements follow.

Additional biographical information on these and other candidates is available at www.ieee.org/organizations/corporate/candidates.htm.

Roger D. Pollard



My vision for IEEE is that it provides such outstanding services to its members that every professional practicing in the disciplines represented by the IEEE Societies will feel that it is essential to be a member. The services that our members regard as most important

are all connected with Technical Activities and are primarily concerned with opportunities to communicate with fellow professionals. The communication may be through writing articles for or reading the technical publications, participation in conferences or electronic communication.

It was as 1998 President of the Microwave Theory and Techniques Society (MTT-S), that I became involved with the Technical Activities Board and realized the importance of

TAB as a forum for the representation of the interests of the Societies and their members. During the last year I have chaired the IEEE's Electronic Products Committee - EPIC, the on-line delivery system due to be launched at the beginning of next year, closely followed by electronic authoring and editorial tools, will have a significant impact on IEEE's ability to add value to its members' intellectual property. Although I have a long record of service at Society level, involvement with TAB activity is only recent. TAB should benefit by having a Chair from outside North America and I offer myself for election because I believe that I can bring some fresh perspective to IEEE Technical Activities.

The key issues that should be at the forefront of the TAB agenda include:

- Technical activities and the Technical Societies are at the heart of IEEE - we must not forget that Society members contribute to and expect to find the most important source of up-to-date, authoritative information that their profession has to offer. Our technical information is the most important service we provide our members in the various forms of publications, conferences, opportunities to meet other practitioners, etc. We must ensure that we maintain and continue to improve the quality for which IEEE technical communications are renowned.
 - It is vital that we recognize the importance of identifying and promoting emerging technologies and providing vehicles for the pioneers to build their communities within a supportive environment of technical professionals.
 - We must strive to increase the participation levels of our mem-
- Continued on next page →*

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For detailed contact information, see the Society Web page: www.sscs.org/info/

For questions regarding Society business, contact the SSCS Executive Office.

Contributions for the January issue of the newsletter must be received by November 3 at the SSCS Executive Office.

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TAB VP-Elect Candidate Statements *continued*

bers by improving the ease and quality of that participation. It is important to act on IEEE's strategic goal of globalization and to make full use of electronic communication to ensure that opportunities to participate are, insofar as is possible, equal in all parts of the world. As examples:

- The authoring and review of articles for IEEE transactions and journals
- Contributing to and attending conferences - we must continue to ensure that our conference venues are accessible to the members
- Involvement in the governance of IEEE - more opportunities to participate at all levels by broadening the base of committee membership
- Delivery of IEEE services
- Leadership in the transition to electronic collection, dissemination and archiving of our intellectual property. The aims must include providing added value to our publishing activity by making full use of electronic means; improving the service to our members (both readers and authors) by timely publication of new material to as wide an audience as possible. We must also ensure that IEEE continues to serve the best interests of its members by deriving a steady revenue stream from the sale of information services.
- It is important that IEEE continues to increase the avenues for recognition of the technical contributions of its members. Although it remains important to recognize lifetime achievements and pioneering work, we must encourage new and innovative awards, especially those directed at the younger members of the profession.

For a professional biography and other details, please look at my personal website (www.imp.leeds.ac.uk/rdp/ieee.htm) or contact me by e-mail (r.pollard@ieee.org) to make any comments or address issues.

Roger Pollard can also be reached at the School of Electronic and Electrical Engineering, The University of Leeds, Leeds LS2 9JT, UK; Phone: +44 113 233-2080; Fax: +44 113 233-2032.

Lewis Terman

I have been a member of TAB for almost 10 years, first as the president of the Electron Devices Society, then as chair of the TAB Technical Meetings Council, two terms a TAB Treasurer, and now as president of the Solid-State Circuits Society and chair of the TAB Strategic Planning and Review Committee. Over the past decade I've also served on a number of TAB committees, including various TAB restructuring and planning committees, and as member and chair of the Society Review Committee, which gave an excellent



opportunity to understand the operations of the various Societies and Councils. Technical activities are key to the IEEE; the technical interchange facilitated by the Society/Council meetings and publications is at the core of the stature and success of the Institute, and the S/Cs account for the majority of IEEE revenues and reserves.

This is an era of dramatic change, and there are a number of important areas which I will focus on:

- *Finances* - financial health is essential for the S/Cs, TAB, and IEEE as a whole. The S/Cs account for well over half the revenue and reserves of the IEEE. The New Financial Model which is being developed within IEEE re-allocates expenses between the various Institute entities, and will have major impact on S/C financials. It is critical that the NFM not impinge on the successful operation of the S/Cs, and that it be accomplished while at least maintaining core member services and controlling costs within IEEE.

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- *Globalization* - the present TAB VP Mike Adler has a strong ongoing effort in making IEEE truly global by involving members from throughout the Institute in its operations, decisions, and activities, both administrative and technical. I fully support this effort, and will continue it.
- *Membership* - there is a large core of potential members which the IEEE has not reached. We have good student membership, and then lose a substantial fraction after graduation. IEEE needs to be made more attractive and relevant to recent graduates, industrial members, and industry in general, while continuing to increase our student membership. Chapters are an excellent vehicle for attracting new members, involving the local technical community, and facilitating interchange and networking at the local level.
- *Intellectual Property* - electronic publication and distribution is in the process of revolutionizing the dissemination of information, and with it the IEEE publication activities. This is going to

have great impact on the IEEE, not only making information readily and quickly available throughout the world, but also potentially affecting S/C and IEEE finances as the traditional publishing model changes. The IEEE must take advantage of this revolution, meet the competition from commercial publishers, and capitalize on the opportunities it offers.

- *Education* - education is one of the areas repeatedly identified as critical to recently graduated members, members changing fields, students, and to the technical community in general. The S/Cs very successfully run many short courses, tutorials, and overviews of new and emerging technical fields. The web offers opportunity to disseminate this information to a much wider audience than can attend the courses. TAB and the S/Cs need to work with the Education Activities Board to make such information widely available.
- *Awards* - a major function of IEEE is the recognition at the Institute level of outstanding technical accomplishment through the Fellow program, and such recogni-

tions as the Technical Field Awards and Institute Medals. However, the TFAs and Medals provide spotty coverage at best for many of the technical areas covered by the S/Cs. This need to be addressed through closer interaction and cooperation with the Awards Board and the Fellows program.

- *Communication* - within the IEEE there are many disparate entities, covering the various facets of IEEE activities and interactions with industry, academia, and the technical community at large. Each such entity has its own focus, agenda, and viewpoint. In addition, IEEE has a professional staff which is very effective in supporting the various activities. It is critical to the success of the IEEE that these groups interact effectively and work together. TAB must have effective and smooth communication with IEEE Corporate and the other IEEE Boards and entities.

Lewis Terman can be reached at the IBM T.J. Watson Research Center, P.O. Box 218, Yorkton Heights, NY 10598; Phone: (914) 945-2029; Fax: (914) 945-1358; E-Mail: l.terman@ieee.org. ●

Events Calendar *continued from page 16*

Technically Cosponsored Meetings

1999 IEEE GaAs IC Symposium

www.gaasic.org

October 17-20, 1999

Monterey Conference Center, Monterey, CA

Deadline for abstracts: past

Contact: Ms. Marie Leonardis

IEEE

1999 IEEE GaAs IC Symposium

445 Hoes Lane

Piscataway, NJ 08855

Tel: (732) 562-3875

Fax: (732) 981-1203

email: m.leonardis@ieee.org

ICVC International Conference on VLSI and CAD

October 26-27, 1999

Hotel Inter-Continental, Seoul, Korea

Summary submission deadline: past

Contact: Youn Choi

SEMI Korea

Korea World Trade Center #4005,

159-1, Samsung-dong, Kangnam-ku,

Seoul, Korea 135-729

Tel: +82-2-551-3404 (ext. 202)

MSICD 1999 IEEE CAS International Workshop on Mixed Signal Integrated Circuit Design

msicd.ece.uci.edu

December 1-3, 1999

Hyatt Hotel, Long Beach, CA

Contact: Dr. Geert De Veirman

Silicon Systems

14351 Myford Rd.

Tustin, CA 92780

Tel: (714) 573-6829

Fax: (714) 573-6916

email: geert.deveirman@tus.ssi1.com

ESSCIRC 2000 European Solid-State Circuits Conference

www.esscirc.org

September 19-21, 2000

Kista Technology Park, Stockholm, Sweden

Paper submission deadline: TBD

Contact: Hannu Tenhunen

Royal Institute of Technology

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Email: Hannu@ele.kth.se

SSCS EVENTS CALENDAR

1999 SSCTC Workshop MEMS Interface Circuits

www.sscs.org/ssctw/oct99/

October 14–15, 1999

Key Bridge Marriott Hotel, Arlington, VA

Contact: Suzanne Demarie

Courtesy Associates

Washington, DC

Tel: (202) 331-2000

Fax: (202) 973-8722

Email: SSCTC@courtesyassoc.com

2000 ISSCC International Solid-State Circuits Conference

www.isscc.org

Monday–Wednesday, February 7–9, 2000

San Francisco Marriott Hotel, San Francisco, CA

Paper submission deadline: Sept. 10, 1999

Contact: Courtesy Associates

Washington, DC

Tel: (202) 331-2000

Fax: (202) 331-0111

Email: ISSCC@courtesyassoc.com

2000 CICC Custom Integrated Circuit Conference

www.his.com/~cicc/

May 21–24, 2000

Caribe Royale, Lake Buena Vista, FL

Paper deadline: Dec. 1, 1999

Contact: Ms. Melissa Widerkehr

Widerkehr & Associates

Gaithersburg, MD

Tel: (301) 527-0902

Fax: (301) 527-0994

Email: cicc@his.com

2000 Symposium on VLSI Circuits

www.bcasj.or.jp/vlsi_sym/

June 15–17, 2000

Hilton Hawaiian Village, Honolulu, HI

Deadline for receipt of summaries: Jan. 7, 2000

Contact: Ms. Melissa Widerkehr

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