Advance Program

Sunday, 3 May 2009

2:30 PM - 5:45 PM

Session TUT: TUTORIAL SESSION
Session Chair: Lukas Chrostowski, *University of British Columbia, Vancouver, BC, Canada*

TUT1 2:30 PM - 3:15 PM (Tutorial)

Weather Micro-Sensors, Weather Modelling and Modification, John Manobianco*, Mano Nanotechnologies, Inc. and AWS Truewind, LLC, Albany, NY, USA*

Technological advancements in micro and nanotechnology have inspired a concept called Global Environmental Micro Sensors (GEMS). The GEMS system has the potential to expand the amount of in situ observations especially over data sparse regions of the Earth and improve weather forecast accuracy and efficiency well beyond current capability. Resulting improvements in forecast accuracy will translate directly into cost benefits for weather-sensitive industries worldwide, and mitigate the risk associated with life-threatening weather phenomena. With a modular sensor suite, GEMS probes could be used to monitor and predict trace gases (ozone, carbon dioxide, etc.) or other parameters of interest for intelligence gathering, battlefield situational awareness, and urban warfare.

This presentation will highlight the body of work on GEMS that has been funded by various entities since early 2001 and conclude with plans for future research and development. The focus will be on the major feasibility issues and the design trade-offs that span a multi-dimensional, interdisciplinary parameter space. Previous conceptual and experimental efforts with GEMS have touched on nearly all of the design issues relating to the conference problem topic of weather modification. The talk will feature aspects of GEMS design, development, and testing directly relevant to these issues.

TUT2 3:15 PM - 4:00 PM (Tutorial)

Participatory Sensing and Its Privacy Concerns, Wenbo He*, University of New Mexico, Albuquerque, NM, USA*

Participatory sensing through mobile and ubiquitous devices (e.g., smart phones) are designed for aggregated information collection with fine-granularity. We expect both social and economic impact of participatory sensing. Applications of participatory networks are likely to deal with highly sensitive or private information. Hence, privacy protection is a critical topic in the design of participatory sensing systems. In this talk, I will first illustrate several applications of participatory sensing and then present the privacy-preserving data aggregation schemes. They are disturbance-based approach, homomorphic encryption approach, cluster-based approach, and Slice-Mix-AggRegaTe (SMART), etc. Finally, we will discuss the trade-offs for achieving privacy, and the general design guideline of privacy-preserving participatory sensing systems.

4:00 PM - 4:15 PM **Break**

TUT3 4:15 PM - 5:00 PM (Tutorial)

Weather Modification, Sigmund Silber, *The New Mexico Weather Modification Association, Santa Fe, NM, USA*

Weather modification can mean different things to different people and can be intentional or unintentional (pollution being a good example which can be interpreted to include greenhouse gas warming).

I will focus on those applications which involve the intentional attempt to increase precipitation which can also result in a reduction in hail, fog, and perhaps even lightning.

The main variables with respect to weather modification relate to when it is performed (summer or winter), the precipitation process that is intended to be modified (type of clouds and where in the cloud), how the precipitation process is intended to be modified (addition of particles, use of shock waves etc), how the modification is transported to where it needs to be (aircraft, rockets, ground release and wind currents) and how the impacts are assessed.

The use of data with regards to weather modification occurs in three very different time frames one being the planning process which can be more or less elaborate, the second being the operational phase where timeliness is critical, and the third being the assessment of results. There can be considerable overlap among these three phases.

The tutorial will explain how weather modification works and the data and methodologies that are utilized in the three phases. I will attempt to discuss both current practice and future opportunities which could be of more interest to this group. I will also discuss atmospheric research that could benefit weather modification and other applications such as research into climate change and flight safety related to icing conditions. There has been some talk regarding the use of weather modification as a technique for Geoengineering to reduce the impact of Global Warming and I will touch on that as well.

TUT4 5:00 PM - 5:45 PM (Tutorial)

A Petascale-Ready Version of the Community Atmospheric Model, Mark Taylor, *Sandia National Laboratories, Albuqeurque, NM, USA*

Climate change is already underway and will accelerate this century, but there are still major uncertainties. Understanding the potential changes and how to mitigate or adapt to them requires high fidelity climate models which simulate many components of the Earth system, including atmospheric and oceanic circulation, land surface processes, sea ice, and chemical and biogeochemical cycles. Modeling these processes at the resolutions needed to accurately assess the regional impacts of climate change will require efficient use of petascale computer architectures. These machines have hundreds of thousands of processors. Effectively using such machines remains a challenge due to several scalability bottlenecks present in all modern climate models. I will give an overview of the Community Climate System Model (CCSM) and then describe some of these scalability bottlenecks. The largest bottleneck is created by the numerical methods used in the dynamical core of the atmospheric model component. I will describe some of the work being done at Sandia National Laboratories to address this issue and make it possible to run the CCSM atmospheric component petascale architectures.

Monday, 4 May 2009

7:55 AM - 8:00 AM **Welcoming Remarks**

Workshop Co-Chairs: Elad Alon, *University of California – Berkeley, Berkeley, CA, USA*
Jon Lexau, *Sun Microsystems, Menlo Park, CA, USA*
Zheng, *Sun Microsystems, San Diego, CA, USA*

8:00 AM - 10:00 AM

Session MA: **OPTICAL INTERCONNECTS**
Session Chair: Xuezhe Zheng, *Sun Microsystems, San Diego, CA, USA*

MA1 8:00 AM - 8:30 AM (Invited)

Optical Proximity Communication and Silicon Photonic Devices - Enablers for the Macrochip Architecture, John. E. Cunningham, Ashok V. Krishnamoorthy, Xuezhe Zheng, Guoliang Li, Ron Ho, Jon Lexau, Ivan Shubin, and Kannan Raj*, Sun Microsystems, San Diego, CA, USA*

We present the macrochip - a computing microsystem that uniquely leverages the bandwidth, density, and latency advantages of silicon photonic interconnect to enable highly compact supercomputer-scale systems. The physical implementation of the macrochip allows one to break the 'single reticle limit' and is a logically contiguous piece of silicon implemented as an advanced WDM point-to-point network. This network offers strictly non-blocking all-to-all connectivity while maximizing bisection bandwidth, making it ideal for interconnecting several core and processors that are far apart from each other. In this talk we introduce the key enablers for the WDM macrochip – namely, the photonic waveguide routers, couplers, and the actives devices. We show that these devices can enable a WDM macrochip network with unprecedented bandwidth-density using optical proximity communications(OPxC) and provide unmatched optical I/O bandwidth density to electrical chips. We show the realization of 10 Gbps optical links using OPxC hops and their broadband operation. We also provide insight on the high-speed performance, area, energy per bit and tuning trade-offs associated with active devices such as high-speed nanophotonic ring modulators and detectors. A key aspect of the implementation is the integration and we show passive alignment techniques for efficiently coupling light in the WDM network.

MA2 8:30 AM - 9:00 AM (Invited)

Review of Optical Interconnect Development in Japan, Kazuhiko. Kurata*, NEC Corporation, Nakahara, Kanagawa, Japan*

Activity in development of optical interconnection is growing in Japan. In this review recent Japanese activities are outlined from an opto-electronics package point of view. Optical interconnection is considered one of the best solutions to realize low power consumption for high data transmission. On the other hand, additional components like optical transceivers and optical connectors are necessary. These components have to be merged in the circuit board without sacrificing board space or the total manufacturing cost. Various concepts of optical components (Optical transceiver, Optical wiring and Optical connector) for optical interconnection are investigated and several components are being developed in Japan: Currently, chip scale optical transceiver is constrained by power consumption of the laser driver IC but the the size of the transmitter will finally reach the limit set by the power consumption of the Vcsel. This limitation might be overcome by CMOS-photonics using on-chip optical modulator. Different types of modulators are currently being discussed. The placement of logic-LSI and optical function in package and optical coupling structure becomes important factor which will be offered in the near future.

MA3 9:00 AM - 9:30 AM (Invited)

The "LightABLE™ Optical Engine" for Hybrid Optical IC Packaging, David. Rolston and Robert Coenen*, Reflex Photonics, Inc., Montreal, QC, Canada*

Processors, switches and other application specific ICs are demanding data rates that are beginning to strain current IC packaging technology. To continue to offer lowcost semiconductor package technology capable of dealing with the i/o bandwidth, power consumption and system size, a hybrid optical IC packaging technology is required. Standard electrical IC packaging techniques are limited in their speed and number of connections to roughly 2-Gbps (DDR) and 1500 connections. However, they are still expected to have a post assembly and test price of less than "a penny a pin". By introducing modular parallel optical modules as another source of i/o for the chip, both data rate and density can be drastically improved. Using a low-cost, modular optical assembly, called the Reflex LightABLE™ optical engine, a standard IC package can be augmented with upto 200 optical channels each operating at 10-Gbps for an aggregate optical i/o bandwidth of up to 2-Tbps. The integration of the optics with the IC package not only offers tremendous speed advantages but also allow a lower overall system power consumption savings. Typical applications for optical i/o directly from the chip allow bus extensions for PCI Express, RapidIO and others, also high-speed data switching systems as well as graphics rendering architectures using extended memories. Also possible are a variety of multipacakge-multiprocessor mesh interconnect architectures.

MA4 9:30 AM - 10:00 AM (Invited)

Optical Interconnection Technology on the Printed Circuit Board Level, Elmar Griese*, University of Siegen, Siegen, Germany*

Novel research results in developing an optical interconnection technology on the printed circuit board level are presented. Apart from different manufacturing technologies for realizing optical layers with integrated optical waveguides also the fundamental waveguides properties which are specific to the corresponding manufacturing process are discussed. The waveguide properties were investigated by a wave theoretical modelling approach which results in a better physical understanding of wave propagation and mode coupling within optical multimode waveguides. Moreover the optical coupling is addressed. Coupling concepts for chip-to-board and board-to-backplane coupling are presented, which take into account accuracy requirements of optical interconnects and existing accuracy and tolerances of conventional printed circuit board technology. This part contains also novel results in developing an optical pin providing a simultaneous bidirectional data transfer at one optical wavelength.

10:00 AM – 10:30 AM **COFFEE BREAK**

10:30 AM - 12:00 PM

Session MB: **Electrical Interconnects**
Session Chair: Elad Alon, *University of California - Berkeley, Berkeley, CA, USA*

MB1 10:30 AM - 11:00 AM (Invited)

Proximity Communication and its Application to Large-Scale Systems, Hans Eberle, Alex Chow, Bill Coates, Jack Cunningham, Robert Drost, Jo Ebergen, Jon Gainsley, Nils Gura, Ron Ho, David Hopkins, Ashok Krishnamoorthy, Jon Lexau, Wladek Olesinski, Tarik Ono, Justin Schauer and Ivan Shubin, *Sun Microsystems, Palo Alto, CA, USA*

I will describe a working prototype of a multi-chip module (MCM) that uses a new chip interconnect technology called Proximity Communication (PxC). With PxC, data is wirelessly transmitted from chip to chip using capacitive coupling. Chips face each other forming micron-sized plate capacitors implemented by the chips' metal layers. PxC circuits rely on precise chip alignment. As part of this talk, I will present a low-cost packaging solution for PxC MCMs that makes this possible through a MEMS-based self-aligning mechanism. PxC is attractive as it offers unparalleled chip IO density allowing the system designer to realize large-scale architectures in ways not possible with conventional technologies.

MB2 11:00 AM - 11:30 AM (Invited)

Trends in High-Throughput On-Chip Crossbar Switches, Ephrem Wu, *LSI Corporation, Milpitas, CA, USA*

On-chip crossbar switches with multiple terabits per second throughput are now feasible. Applications include multi-core system-on-chips and high-throughput switches and routers. We will discuss how new on-chip switch architectures work around the negatives and exploit the positives of process technology trends.

MB3 11:30 AM - 12:00 PM (Invited)

High-Speed Flex-Circuit Off-Package Interconnect, Henning Braunisch, *Intel Corporation, Chandler, AZ, USA*

We present results from high-speed chip-to-chip interconnect prototypes utilizing flex-circuit technology for extending the lifetime of copper-based system-level channels. Proper low-loss construction of the flex ribbon is shown to improve raw bandwidth over standard FR-4 boards by three times. Active testing results from a 130-nm CMOS test vehicle show the potential of up to two times higher signaling rates. The next-generation 90-nm CMOS circuits give improved voltage and timing margins at 20 Gb/s. In an interconnect limited case a channel with 36 in (91.4 cm) of flex runs at 18.2 Gb/s signaling rate at a bit-error ratio of better than 10^{-12}. The channel includes two 90-nm CMOS test chips, two organic flip-chip package substrates, and two custom flex connectors; crosstalk is not included in this experiment. High-speed connector solutions, including results from a “split socket” assembly test vehicle, are discussed in detail. The characterization of two top-side flex connector prototypes demonstrates their basic durability and good high-frequency performance, including cross-talk.

12:00 PM – 12:15 PM **Workshop Problem Statement**
Lukas Chrostowski, *University of British Columbia, Vancouver, BC, Canada*

12:15 PM – 1:45 PM **Luncheon & Working Group Session I**

1:45 PM – 3:45 PM **Working Group Session II**

6:00 PM – 7:30 PM **Welcome Reception - Chamisa Courtyard**

Tuesday, 5 May 2009

8:00 AM - 10:00 AM

Session TuA: **INTERCONNECT-CENTRIC SYSTEMS**
Session Chair: Frederick B. McCormick, *Sandia National Laboratories, Albuquerque, NM, USA*

TuA1 8:00 AM - 8:30 AM (Invited)

Data Movement Dominates: An Application-Centric View of High Performance Interconnects, Richard. C. Murphy, K. Scott Hemmert, Brian Barrett and Arun F. Rodrigues*, Sandia National Laboratories, Albuquerque, NM, USA*

In an era where moving bits to a computation unit expends more energy than the computation itself, and supercomputer application performance is dominated by interconnect at all levels (functional unit-to-functional unit, chip-to-chip, board-to-board, and cabinet-to-cabinet), this talk will present a synthesis of results describing application requirements and interconnect construction methodologies. Two classes of applications will be considered: traditional "physics" codes that simulate the evolution of physical systems, and thus display structure that can be exploited by network topologies; and "informatics" applications that look at real world data or the output of simulations to derive knowledge from data (in the formation of a hypothesis, etc.). The talk will examine the power, performance, and economics of constructing a supercomputer, and the demands that those optimizations place on interconnect at all levels. This will be done in the context of both traditional commodity Massively Parallel Processing (MPP) systems, that typically have highly custom system interconnects, and the trade-offs enabled by more custom machines. The talk will end with a strawman architecture currently under examination at Sandia.

TuA2 8:30 AM - 9:00 AM (Invited)

Requirements for Data Center Interconnects, Bikash Koley*, Google Inc., Mountain View, CA, USA*

ABSTRACT NOT AVAILABLE

TuA3 9:00 AM - 9:30 AM (Invited)

Implementing Photonic Interconnections in Space: Opportunities and Challenges, Davis H. Hartman*, General Dynamics, Scottsdale, AZ, USA*

Space-borne information gathering systems are overwhelmed by data volume. Signal processing techniques that thin data are very critical to these systems. Three fundamental trade parameters drive the design of these complex leading-edge systems. These are (1) performance, (2) reliability and (3) cost. In most designs, one can get two of these parameters, but at the cost of the third. In the commercial world, computer markets are driven by low cost and high performance metrics. While high reliability is desirable, the steep cost learning curves of commercial markets do not reward high reliability. In space or avionics based military markets, the trade tends to favor high performance and high reliability. The most effective way to control system cost is to minimize size, weight and power (SWaP). On average, it costs $10,000 per kg and $6,000 per Watt to launch a high performance payload into a low earth orbit (LEO) in space.

In this presentation, we discuss a class of space-based reference systems for which photonics can benefit the performance/reliability/cost trade through SWaP reduction. We discuss roles for photonics to augment electronic interconnects in such systems, along with their ability to scale favorably in SWaP as information volume and data bandwidth grow unbounded.

TuA4 9:30 AM - 10:00 AM (Invited)

Interconnect Requirements for Exascale Computing, Peter M. Kogge*, University of Notre Dame, Notre Dame, IN, USA*

A recent study of the technology requirements for exascale computing determined that power is the first of four major challenges. This talk will discuss theses challenges, especially power, with a primary emphasis on interconnect. A detailed analysis of the energy costs of accessing operands from different possible sources within a high speed system (done since the study) will be used to demonstrate the high cost of interconnect in the overall process of delivering values to function units, even when very advanced interconnect protocols are assumed.

10:00 AM – 10:30 AM COFFEE BREAK

10:30 AM - 12:30 PM

Session TuB: **EMERGING TECHNOLOGIES**
Session Chair: Tian Gu, *University of Delaware, Newark, DE, USA*

TuB1 10:30 AM - 11:00 AM (Invited)

100GbE with Si Photonics, Mehdi Ashgari*, Kotura, Monterey Park, CA, USA*

ABSTRACT NOT AVAILABLE

TuB2 11:00 AM - 11:30 AM (Invited)

100GbE from IEEE and ITU Perspective, Francesco Caggioni*, AMCC, Andover, MA, USA*

Over the past couple of years ITU, IEEE and OIF have actively worked toward a common goal of enhancing the capability of the Network toward 100G interconnects. It is clear that convergence between Telecom and Datacom is happening at many levels. In this presentation some of the important changes coming in Ethernet Architecture (important for scalability) and ITU Hierarchy (Important for Convergence) are presented. Technology in Electrical Signaling and Optical Communication have "evolved" over the past many years but as roadblocks to evolution come up, signs of revolutionary technology start to appear at the horizon, some of these promising technologies and problems will be presented.

TuB3 11:30 AM - 12:00 PM (Invited)

Comb Laser Transceiver Strategies for WDM Computer Interconnects, Alexey Kovsh, G. Wojcik, D. Yin, *Innolume, Inc, Santa Clara, CA, USA*, Alexey A. Gubenko, Igor L. Krestnikov, Sergey S. Mihkrin, Daniel A. Livshits, *Innolume GmbH, Dortmund, Germany*

Wavelength-division multiplexing (WDM) multiplies telecom bandwidth by injecting many modulated wavelengths into each fiber. It is limited to WANs and MANs today but is moving into access networks via WDM-PON. Migration to computer communications (compcom) reaches, i.e., into LANs, server farms, and ultimately computers, is hampered by complexity and cost of WDM systems. VCSEL-driven parallel optics is today's compcom alternative but its proliferation of underutilized fiber is ultimately self-limiting. In fact, IBM recently suggested that low-cost, short-reach WDM rather than parallel optics is needed to sustain commercial growth of their HPC business. Therefore, system designers must find ways to incorporate cost-effective WDM at compcom reaches but at dramatically reduced cost, by perhaps 4+ orders of magnitude. One significant impediment to downscaling and commodifying WDM is the multi-wavelength laser sources required. Today's options include laser arrays on InP or bonded to silicon. A better alternative is a diode comb laser based on InAs/GaAs quantum dots (QDs). This single laser is a viable WDM source because its low RIN permits external modulation of each longitudinal mode (channel) at 10+ Gb/s, and it operates within telecom's O-band. Transceiver issues and implementations need to be explored aggressively and we describe the current state-of-play.

TuB4 12:00 PM - 12:30 PM (Invited)

Biosensors for POC Applications, Hua Wang*, California Institute of Technology, Pasadena, CA, USA*

Future Point-of-Care (PoC) molecular-level diagnosis requires advanced bio-sensing systems that can achieve high sensitivity and portability at a low power consumption all within a low price-tag. To address this application, an ultra-sensitive frequency-shift based sensor scheme is proposed to detect magnetically labeled biomolecules without using expensive post-processing steps or external biasing permanent- or electro-magnets. The sensor scheme is implemented as an 8-cell sensor array in a standard 130nm CMOS process. With a frequency-shift resolution better than 0.13ppm, the sensor successfully detects both one single magnetic bead (D=1μm) and 1nano-molar physical DNA samples labeled by magnetic nanoparticles.

12:30 PM – 2:00 PM	**Luncheon & Working Group Session III**
2:00 PM – 4:00 PM	**Working Group Session IV**
4:00 PM – 7:30 PM	**Free Afternoon**
7:30 PM – 8:30 PM	**Student Poster Session**
8:30 PM – 9:00 PM	**Presentation of Workshop Problem Solutions**

Student Poster Presentations

Printed Circuit Board based Modulated Retroreflector using Three Large-Area Quantum Well Modulators, Rohit Nair and Keith W. Goossen, *University of Delaware, Newark, DE, USA*

Modulated retroreflectors (MRRR) have several military and commercial applications which include low-power communication with ultralight air vehicles, space-to-ground optical communication, terrestrial point-to-point free space optical communication, remote telemetry, remote sensing of hazmats, distance measurement, dynamic optical tags for equipment and personnel and potentially, on-road vehicle-to-vehicle communication for accident preventions. For communication applications, the MRR's can have advantages over radio links in terms of power dissipation and selectivity. The applications listed above and others require the construction of three dimensional optics and electronics with optical precision.

Variable Swing Optimal Parallel Links – Minimal Power, Maximal Density for Parallel Links, Claudia P. Barrera, Fouad Kiamilev and Nick Waite, *University of Delaware, Newark, DE, USA*.

The rapid growth of chip to chip interconnect density, speed, and the demand for smaller and more portable devices has taken the signal integrity engineers to the limits of PCB (Printed Circuit Board) design. Special care has to be taken in the design stage to guarantee that noise specifications are met and power specifications and geometry of the links ensure minimal crosstalk noise in the system.

Plastic Optical Fiber Embedded Directly into Printed Circuit Boards for Parallel Optical Interconnection Applications between Chips, Michael E. Teitelbaum and Keith W. Goossen, *University of Delaware, Newark, DE, USA*.

For electrical lines, interconnects between chips become increasingly problematic as the length of the interconnect increases. When using optics however, the length of interconnects is not really as issue. For this reason much research has been performed on integrating waveguides directly into printed circuit boards (PCB). However, no one technology has emerged as the clear winner for accomlplishing the goal. In the work herein, a method of integrating plastic optical fiber (POF) directly in to a PCB through mechanical grooving processes is presented. With this method a TIR mirror is also integrated into the POF using mechanical machining methods that are compatible with current PCB manufacturing techniques. The validity of the technique was tested experimentally as well as simulated using Monte Carlo ray tracing.

Analytical Energy and Bandwidth Model for Compact Silicon Photonic Microdisk Resonators, William A. Zortman, Michael R. Watts and Douglas C. Trotter, *Sandia National Laboratories, Albuquerque, NM, USA*.

Microdisk resonators for use as low energy modulators in telecom and datacom applications have been fabricated using vertical PN junctions which operate in reverse bias. These devices have demonstrated the lowest energy/bit thus far. In this paper we show that the reverse biased PN junction diodes follow the analytical depletion approximation based on numerical simulation.

Modulator-based Surface-Normal Optical Sources for Intrachip Optical Interconnects, Tian Gu and Michael W. Haney, *University of Delaware, Newark, DE, USA.*

The work presented here introduces vertically emitting optical sources that are based on multiple quantum well modulators (MQWMs).

Wednesday, 6 May 2009

9:00 AM - 11:30 AM

Session PLE: PLENARY SESSION
Session Chair: Gu-Yeon Wei, *Harvard University, Cambridge, MA, USA*

PLE1 9:00 AM - 9:45 AM

Hybrid Silicon Photonics, John E. Bowers, *University of California - Santa Barbara, Santa Barbara, CA, USA*

The evolution of optical networks is requiring increasing complexity in photonic integrated circuits (PICs), together with continual pressure to reduce the cost and power consumption of PICs. Silicon CMOS foundries have the maturity and process control to allow larger PICs with greater yield and reliability with substantially lower cost. Recent developments have allowed the premier performance of passive silicon PICs to be integrated with active components for optimum results. This will allow new markets and opportunities to be exploited for both higher performance and high volume applications. Low cost photonic circuits are essential for future on chip and off chip interconnects to solve the communication and power bottlenecks in multicore architectures.

BIO: John E. Bowers is Director of the Energy Efficiency Institute and a professor in the Department of Electrical and Computer Engineering at the University of California, Santa Barbara. He is also CTO and cofounder of Aurrion and Chairman of the Board of BioIQ. Prof. Bowers is cofounder of Calient Networks and Terabit Technology (sold to Ciena). His research interests are primarily concerned with silicon photonics, optoelectronic devices, optical switching and transparent optical networks. Prof. Bowers received the M.S. and Ph.D. degrees from Stanford University. He worked for AT&T Bell Laboratories and Honeywell before joining UCSB.

Dr. Bowers is a fellow of the IEEE, OSA and the American Physical Society, and a recipient of the IEEE LEOS William Streifer Award and the South Coast Business and Technology Entrepreneur of the Year Award. He was an elected member of the IEEE LEOS Board of Governors, a LEOS Distinguished Lecturer, and Vice President for Conferences for LEOS. He has published eight book chapters, 450 journal papers, 700 conference papers and has received 52 patents. He is a member of the National Academy of Engineering. He and coworkers received the ACE Award for Most Promising Technology for the hybrid silicon laser in 2007.

9:45 AM - 10:00 AM **COFFEE BREAK**

PLE2 10:00 AM - 10:45 AM

Ultra-High-Frequency-Electronics, Mark J. W. Rodwell, *University of California - Santa Barbara, Santa Barbara, CA, USA*

ABSTRACT NOT AVAILABLE

BIO: Mark Rodwell is Professor in the Electrical and Computer Engineering Department at UCSB. He also directs the UCSB Nanofabrication laboratory and its participation in the NSF National Nanofabrication Infrastructure Network (NNIN). He received his Ph.D. in Electrical Engineering from Stanford University in 1988. He worked at AT&T Bell Laboratories during 1982-1984.

His research group works to extend the operation of electronics to the highest feasible frequencies. Their research thus includes semiconductor devices (diodes, transistors, photodiodes), semiconductor fabrication process, circuit design, interconnects, instruments, and communications systems.

Particular interests include InP bipolar transistors, III-V ICs operating above 100 GHz, and high frequency IC design in both III-V and Silicon VLSI technologies. His group's work on GaAs Schottky-diode ICs for subpicosecond/mm-wave instrumentation was awarded the 1997 IEEE Microwave Prize. Prof. Rodwell was elected IEEE Fellow in 2003.

PLE2 10:45 AM - 11:30 AM

TBD

11:30 AM – 11:45 AM **Closing Remarks**