Guest Editorial
Introduction to the Special Issue on 2006 International Integrated Reliability Workshop (IIRW)

I. Introduction

THE PAPERS in this Special Issue of IEEE TDMR were selected from the International Integrated Reliability Workshop (IIRW), which was held on October 16–19, 2006 at the Stanford Sierra Camp on the shores of Fallen Leaf Lake near South Lake Tahoe, CA. This annual workshop, which was sponsored by the IEEE Reliability Society and the IEEE Electron Devices Society, provides a unique forum for open and in-depth discussions of all areas of semiconductor reliability research and technology.

Unlike typical technical-presentation-focused conference, the setting of IIRW encourages the interaction among all attendees. Attendees stay in cabins without televisions or phones, dress is casual, and meals are provided at the family-style lodge dining room. Attendees are expected to participate actively and are drawn into technical discussions from the start. Days are packed with oral presentations and short courses, whereas evenings are spent in reliability discussion groups, poster sessions, and special interest groups. The fresh mountain air can stimulate discussions late into the night.

The collection of articles presented here is intended to provide a flavor of the results presented and discussions held at the workshop and should be of great interest to anyone working on all aspects of advanced MOS device, circuit, and material reliability. In addition to this special proceeding issue, the workshop also publishes a Final Report.

II. Editorial Preview

There are 14 invited papers in the Special Issue on 2006 IIRW. The first two papers focus on device reliability, followed by four papers on back-end reliability, two papers on wafer level reliability (WLR), three papers on memory reliability and e-fuse reliability, along with two papers on high-κ, and the final paper on electrostatic discharge (ESD).

J. M. Roux, D. Roy, and P. Abramowitz of STMicroelectronics and X. Federspiel of Philips investigate the impact of self-heating on the Hot Carrier Injection (HCI) lifetime prediction for silicon-on-insulator technology. Based on their study, a method is proposed to correct the HCI data set from self-heating contributions and thus obtain an accurate estimate of HCI lifetime prediction.

C. Guerin, A. Bravaix, and M. Denais of STMicroelectronics and V. Haurd of Maisondes Technology focus on the Channel Hot Carrier (CHC) degradation mechanisms in nFETs at the 45- and 65-nm nodes. This study applies both the charge pumping and direct-current current–voltage (I–V) measurement methods to determine the density and spatial extent of the interface traps and thereby shows that there are two different CHC degradation regimes, which depend on the gate voltage (V_g). The study also highlights the need for relevant model that would take into account the high V_g regime.

The next four papers focus on reliability problems in back-end including capacitors and resistors in mixed signal applications.

X. Federspiel and L. Doyen of NXP Semiconductor combine physical analysis of failed parts with in-depth analysis of resistance evolution in dual damascene Cu lines subjected to electromigration stress. From this analysis, they extract an activation energy from single samples as well as information about liner properties and the fabrication process.

A. Bajolet, S. Bruyere, and M. Proust of STMicroelectronics and L. Montes and G. Ghibaudo of the Institut de Microélectronique, Electromagnétisme et Photonique examine the impact of TiN posttreatment on charge trapping in alumina layers in a 3-D MIM capacitor. Comparison of chemical vapor deposition and physical vapor deposition TiN process effects on the alumina layer is discussed.

G. Groeseneken, K. Maex, and Z. Tokei of the Interuniversity MicroElectronics Center (IMEC) analyzed conduction mechanisms in advanced low κ by means of intermittent capacitance measurement during voltage stress. They evidenced changes of the donor/acceptor densities from I–V curve slope evolution aside from dominant bulk conduction.

Analog Devices investigates wear-out mechanisms in SiCr resistive devices under constant current stress. An accurate analysis of resistivity and TCR was performed to obtain a fair comparison of devices issued from different production sites and to establish robust design rules. Additionally, a physical origin to the resistance changes detected during wear out is proposed.

The two WLR papers focus on electromigration and time-dependent dielectric breakdown (TDDB).

O. Aubel of Advanced Micro Devices and T. D. Sullivan, D. Massey, T. C. Lee, T. Merrill, P. Polchlopek, and A. Strong of IBM present various normalization procedures applicable to wafer level electromigration tests, including cross-section and TCR corrections. Using these procedures, the authors analyzed

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the evolution of electromigration activation energy as a function of linewidth.

The second paper is from A. Aal of Elmos Semiconductor AG. The author presents a method to generate TDDB data with high accuracy from linear ramped voltage test. Such a method is very useful for performing fast lifetime projection for gate oxides. Compared to conventional constant-voltage-stress-based TDDB tests, the new method offers a much faster test, resulting in reduced costs for process qualification and WLR monitoring.

The following three papers review reliability issues associated with NiSi polycide e-fuses and embedded Flash memory reliability.

S. Tumakha, J. Im, and S. Paak of Xilinx describe e-fuses in the 65-nm node. Optimal programming stimulus and mechanisms are described, and a study on the limitations of reliability for unprogrammed e-fuses versus read current limits is discussed.

S. Mori, M. Kanno, and N. Nagashima of Sony investigate dopant-dependant e-fuse properties. A discussion of the current flow and its effect within the silicide layer and the polysilicon layer is analyzed.

G. Tao, H. Chauveau, and S. Nath of NXP Semiconductors study the endurance of a 2T-FNFN NOR Flash memory cell that is embedded in a 0.13-μm technology node. An empirical model describing the degradation in the program window as a function of temperature is described.

In the final papers of the Special Issue, focus is shifted to high-κ reliability.

S. Jakschik, M. Kerber of Infineon, Th. Kauerauf, R. Degreave of IMEC, Y. N. Hwang of Samsung, R. Duschl, A. Avellan, and S. Kudelka of Qimonda discuss the influence of stress-induced leakage current in HfSiO devices under substrate injection conditions. Most of the degradation was attributed to damage in the high-κ layer and not at the interface with silicon.

J.-P. Manceau, S. Bruyere, and S. Jeannot of STMicroelectronics, A. Sylvestre of LEMD, and P. Gonon of LTM investigate the current instability and permittivity variation with frequency for Ta_2O_5 capacitors, where three types of phenomena are observed, namely: 1) polarization current; 2) Poole–Frenkel conduction; and 3) a resistance degradation phenomenon. A model for oxygen vacancy migration is also proposed.

The last paper of this Special Issue is by W.-J. Chang and M.-D. Ker of National Chiao-Tung University, who investigate the dependences of device structures and layout parameters on ESD robustness in 40-V CMOS chips and conclude that the high-voltage MOSFETs without drift implant in the drain region have better transmission line pulsing-measured It2 and ESD robustness.

The cross section of the work presented at IIRW that appears in this issue should allow the reader to come away with a deeper understanding of the latest reliability challenges.

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