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SOLID-STATE CIRCUITS

IEEE Solid-State Circuits Society Quarterly Newsletter



Symposium on VLSI Circuits Meets in June

Wai Lee, *Symposium on VLSI Circuits Publicity Chair, lee@ti.com*

The International Symposium on VLSI Circuits will be held on June 16-18th, 2005 at the Rihga Royal Hotel, Kyoto, Japan. The Symposium consists of three days of technical presentations and informal evening rump sessions on VLSI circuit design. Following tradition, the Symposium on VLSI Circuits will follow the Symposium on VLSI Technology at the same location.

The Symposium will mark its 19th anniversary this year. The Symposium has established itself as a major international forum for presenting and exchanging important ideas and new

developments in VLSI circuit design. The scope of the Symposium has been expanded to include new concepts in VLSI design, such as MEMS, novel memory, quantum computing, in addition to the traditional analog, digital, memory, signal processing, and communication circuits. The circuit innovations to be presented at this Symposium will form the foundation for future developments in portable and desktop computing, game consoles, portable communication equipment, digital cameras and imaging devices, wireless LAN and wireline communication infrastruc-

ture equipment, as well as biomedical devices. Contributions to the Symposium come from both industry and academia around the world.

This year the technical program committee reviewed 259 submissions to the conference and chose 92 papers for presentation and publication at the Symposium. This large number of top-quality technical papers results in a technical conference that will be bigger and better than ever. That is why you do not want to miss this unveiling of unprecedented technical papers, featuring new and innovative demon-

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Asia Launches New Solid-State Circuits Conference

Nov 1-3, 2005 in Hsinchu, Taiwan

The new Asia Solid-State Circuits conference (A-SSCC) will hold its inaugural meeting 1-3 November this fall in Hsinchu, Taiwan. Endorsed by the IEEE Solid-State Circuits Society as a fully sponsored conference, the A-SSCC will also leverage the interest of local industry to ensure a successful conference.

The A-SSCC will influence the growth of the design industry in Asia and serve as a platform for regional cooperation. Asia is already recognized as a major chip manufacturing power house, with proven world-class foundry expertise. Asia is also the destination of huge consumer markets for electronic products. With the new phase of the integrated VLSI industry, the time is right for the launch of this new SSCS conference.

Besides the convenient location to attract the local design talent, Asia's

technology strengths make the conference a global destination. Low-power/low-voltage CMOS, memory circuits, relevant device technology, and circuits and devices for hand-held equipment and display are all leadership areas of Asian industries.

A key trait of the new conference will be a practical industry program, one-third of the program according to organizers goals. Product-based presentations will include specifications, applications, and live demos. Papers will point out advances to the state-of-art, circuit improvements, chip photos, characterization results and packaging/testing results. The subjects will include both chip architecture and software.

A special section of an issue of the JSSC will be dedicated to extended versions of papers from

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strations of leading-edge concepts.

About the Venue

The Rihga Royal Hotel is located in Kyoto, the old capital of Japan, which attracts many visitors from all over the world. The JR Kyoto station was totally renovated and modernized in 1997, so now you can enjoy the combination of a modern station building along with the traditional Kyoto cityscape. For further information, please visit the Web site of the Kyoto Convention Bureau (which also provides a look at the history and culture of Kyoto) at web.kyoto-net.or.jp/org/hellokcb/index.html.

Technical Highlights

Papers to be presented at the Symposium will cover the latest and interesting circuit design concepts for digital, memory, analog, wireless, and wire-

line applications. The highlights include the first DDR3 DRAM operating at 1.6 Gb/s/pin, the highest performance ARM processor operating at 1.5 GHz using a 90nm process, a CMOS ultra-wideband (UWB) transceiver using impulse radio technique to achieve a data rate of 1Mbps, a 14bit digitally self-calibrated pipelined ADC with adaptive bias optimization for arbitrary speeds up to 40MS/s, and a digitally programmable 3-tap transversal filter in 90 nm CMOS for equalization up to 30 Gb/s.

Invited Speakers

Invited papers are always the high point of the Symposium, focusing on both technical and business implications of technology changes, presented by academic and industry leaders. This year we will have four distinguished speakers. On June 16, Dr.

Kotaro Sabe of Sony will present a paper on "Development of entertainment robots and robotics future," and Mr. John McCorkle of Freescale Semiconductor will give a presentation on "Ultra Wide Band (UWB): Gigabit wireless communications for battery operated consumer applications." On June 17, Dr. Mohammad Mojaradi of NASA and JPL will discuss "Design challenges and methodology for developing new integrated circuits for the robotics exploration of the solar system" and Dr. Yun-Seung Shin will describe "Prospects and challenges of flash memory for mobile/consumer applications."

Rump Sessions

Evening rump sessions are organized around controversial topics and experts are invited to present their divergent views. All aspects of the controversy are explored, and a spirited discussion ensues; active audience participation is encouraged! This year the rump session topics for the Circuits Symposium are:

- Low power design: process puzzle or design dilemma?
- The roadblock to the TeraBit (1012 bits) memory era: is it technology or design?
- Digitizing the radio to the antenna: will radios still need analog in 2010?

These rump session topics give a good idea of controversies plaguing the industry. What are the roadmaps for future device technology and circuit design techniques that can allow the industry to continue to deliver higher performance with a shrinking power consumption budget? What storage technologies and/or circuit design techniques will allow us to go beyond 100 Gb/chip memory density in the next decade? Will the demand of single-chip implementation and high-level of integration force all radio functions to be implemented in digital circuits, rather than by traditional analog techniques?

Overlap Day

A special feature of the Symposium is the one-day overlap in the schedules for the International Symposium on

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For detailed contact information, see the Society Web page: www.sscs.org

For questions regarding Society business, contact the SSCS Executive Office.

Contributions for the July 2005 issue of the e-News **must be received by 16 June 2005** at the SSCS Executive Office.

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VLSI Technology and the Symposium on VLSI Circuits. This is an excellent opportunity to meet with members of the opposite discipline to share experiences, issues, and ideas for future improvements. In addition, there is also a joint rump session organized by members of both the Circuits and Technology committees. This year's topic is "Who will conquer the issues of variability? Will technology people be able to keep the device variability? Will design technology take the device variability into account?"

VLSI Circuits Short Course

Prof. Makoto Nagata of Kobe University and Dr. Vivek De of Intel

Corp. have organized an excellent one-day Short Course entitled "Multi-GHz clocking technologies for microprocessors" on Wednesday, 15 June. Experts in the field will cover:

- Basics of clock delivery
- Components of clock generation and distribution
- Methodologies for high-performance and low-power applications
- Techniques for synchronizing multiple clock domains

This Short Course is condensed to one-day to give attendees an excellent overview of the topic as well as to provide the latest developments in the area. This is a rare opportuni-

ty to hear timely presentations describing work in a technical area given by recognized leading practitioners and researchers who teach others to do what they do best.

Further Information

For questions about hotel reservations contact:

Rihga Royal Hotel Kyoto
Horikawa-Shiokoji, Shimogyo-ku,
Kyoto 600-8237, Japan
Tel: +81-75-341-1121
Fax: +81-75-341-3073

For registration and other information, visit the VLSI Symposia home page at: www.vlssymposium.org. ●

SSC Conference Digital Library Has Member Appeal

Anne O'Neill, SSCS Executive Director, a.oneill@ieee.org

The SSC Conference Digital Library is a subscription to the Digests of SSCS sponsored conferences via IEEE *Xplore*. Offered for the first time in 2003, there has been a 20% increase in subscribers each year while the rate has remained at \$75. Presentations are available as soon as the Digest pdf files are posted in *Xplore*.

Articles are available for all SSCS sponsored conferences from their inaugural meeting. ESSCIRC, for which SSCS provides technical co-sponsorship, will have articles going back to 1997, posted online this summer. For current subscribers, access is provided to these four conferences:

- a) ISSCC, International Solid-State Circuits Conference from 1955
- b) VLSI, Symposium on VLSI Circuits from 1988

- c) CICC, Custom Integrated Circuits Conference from 1988
- d) ESSCIRC, European Solid-State Circuits Conference from 2003

DVD Versus Online Library

There is a DVD version of these conference files. The SSC Digital Archive offers all the same conference files on disk for a one time fee of \$140 and allows researchers to work untethered. However many users see advantages to the online subscription. First, all new conference Digests are available as soon as they are posted. You don't have to remember to place an order for current year conference Digests throughout the year. One \$75 fee for the online access is typically half the cost of a CD version of a single conference Digest. You don't misplace an online subscrip-

tion as you can a disk, or have it at work when you need it at home.

And with the launching of *Xplore* version 2.0, each conference has its own home page for easily locating and searching all the conferences history.

Beginning in 2006 the new A-SSCC conference will be included in the access rights, resulting in a list of the five major circuits conferences.

Members who have access to IEEE *Xplore* or the IEL through their employer or campus, or through their own IEEE Member Digital Library, should verify if they already have access to conference files before paying again for this member subscription.

To subscribe to the SSC Conference Digital Library, members can add services online www.ieee.org/addservices. ●

Conferences Have Home Pages in Xplore 2.0

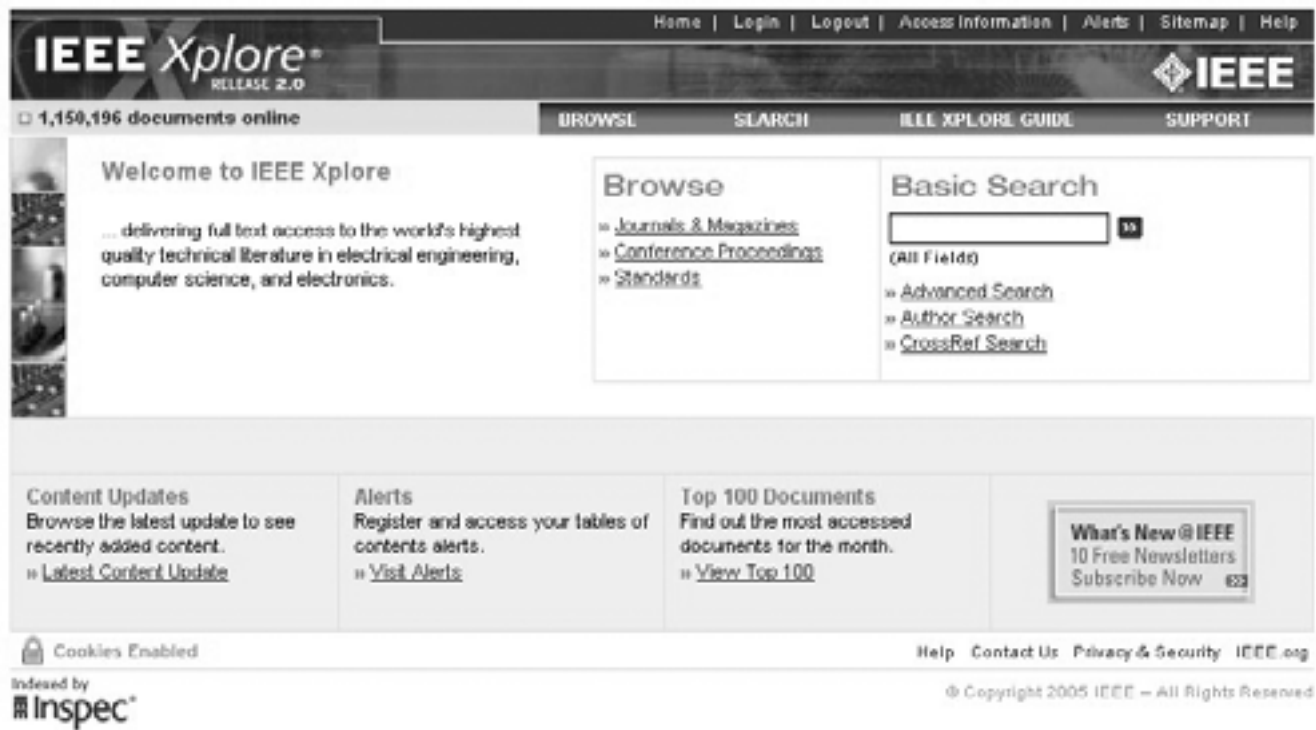
Top 100 IEEE Articles Featured

IEEE *Xplore* Version 2.0, launched 26 March 2005, provides a home page for each of your favorite integrated circuit conference proceedings. All the years of the conference digest are consolidated on a single page, listed just like journals. From this page a user can key in a topic or author to easily search the

history of all the conference proceedings. Also nicknames or acronyms can now be used to find conferences using the BROWSE function. Try "ISSCC" or "VLSI Circuits." Many conference digest links on the sscs.org pages have been revised to go straight to conference home pages in *Xplore*. Use the SSC Con-

ference Digital Library for direct links to ISSCC, VLSI, CICC and ESSCIRC. sscs.org/pubs/conf-dl.htm

The "Top 100 Articles" from the *Xplore* 2.0 home page links to a list of the most frequently downloaded articles in the past month. Since the *JSSC* has more hits than any of IEEE's publications, top



JSSC articles will always be listed there. But the full list offers a fascinating view of current and changing technical interest. For the March launch listing, the December 2004 JSSC article by Bevilacqua and Nikneiad, “An ultrawideband CMOS low-noise amplifier for 3.1-10.6-GHz wireless receivers” was among the top 10. Additional frequent downloads included IEEE standards 801.16.4, 802.16, 802.11, and 802.3ae and a 2003 ESSCIRC article on “A novel universal battery charger for NiCd, NiMH, Li-ion and Li-polymer.” For subscribers behind in their reading, information about which articles most others read can save time when catching up.

The release of *Xplore* 2.0 marks a milestone in the evolution of the IEEE's web delivery platform because it adds not only an updated graphic design, but also adds many new functions to improve the user's experience and facilitate web-first publishing. IEEE *Xplore* is already widely used: during the first two months of this year the users retrieved 4.55 million documents a month -- an increase of 25% over the first two months of 2004. We expect these enhance-

ments will help further increase the use of IEEE's superb technical information.

Key Improvements in Xplore 2.0 include:

A new home page that makes it easy to immediately access information.

Free Basic Search for guests (guests only get to see basic abstracts for free as a result of their search)

Improved search

- Search full-text now fully integrated (no longer a prototype) - - it's a user selection from the search screen
- Search just within the latest content update (so it is easier to see just what's new)
- Search session history (so you can review and combine previous search results from your current session)
- Mark items on search results for easier download to citation manager tools, for printing or emailing citations

Expanded journal and magazine “homepages” better identify each periodical and provide easy access to everything about it.

- Cover images and publication

logotype

- Full information on scope, editorial boards, contact info for editor, etc.
- Sponsoring IEEE Societies links plus Society logos
- Immediate link to table of contents for current or previous issues
- Manuscript Central links for journals that use this service for author submission
- Links to subscription information
- References presented at the search results page
- Browse recent issues right from the periodical's home page
- “Email to a friend” function to send abstracts to a colleague

Improved abstracts records

- Author keywords for titles where available, in addition to Inspec index terms
- DOI display
- Online posting date display (especially useful for publications that post online before print)

An improved single-article purchase process

Improved support

- Fully integrated IEEE Xplore Guide
- IEEE Xplore demo tutorial
- OPAC linking for librarians ●

Asia Launches New Solid-State Circuits Conference

Continued from page 1

A-SSCC. Speakers from ISSCC will be invited to present at A-SSCC, in order to provide highlights from the SSSC flagship conference.

The venue will move around sites in Asia. Scheduled for November, the A-SSCC will be the last major circuit design conference each year. Future meetings are planned for China, Korea, Japan, India and Singapore. The A-SSCC has used 6 years of experience of the Asia-Pacific ASIC (AP-ASIC), a rotating SSSC Chapters conference, to help expand and clarify the goals for the new A-SSCC. The ratio of number of manuscripts submitted to the number of select-

ed has improved during the life of the AP-ASIC so that high quality papers are anticipated for the first A-SSCC.

The A-SSCC has put together a visionary and knowledgeable international steering committee.

- Chair: Chong-Kuang Wang, NTU, Taiwan
- Secretary: Shen-Iuan Liu, NTU, Taiwan
- Kunihiro Asada, University of Tokyo, Japan
- Navakanta Bhat, Indian Institute of Science, India
- Anantha Chandrakasan, MIT, USA
- Genda Hu, TSMC, Taiwan
- Kiyoo Itoh, Hitachi Central Research, Japan

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- Sung Bae Park, Samsung Electronics, Korea
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- Willy Sansen, KUL, Belgium
- Kazuhiro Shimohigashi, Semiconductor Technology Academic Research Center, Japan
- Jyuo-Min Shyu, ITRI, Taiwan
- Hoi-Jun Yoo, KAIST, Korea
- Zhihua Wang, Tsinghua University, China

The conference URL is www.a-sscc.org/

Chapters Report

Denver Chapter News

Alvin Loke, Chair,
alvin.loke@iecc.org and
Tin Tin Wee, Secretary/Webmaster,
tintin.wee@iecc.org

In the past four months, the SSSC Denver Chapter hosted meetings spanning technology, device, reliability, and design topics. In December 2004, newly elected chapter chair Dr. Alvin Loke of Agilent Technolo-

gies presented a tutorial on deep submicron CMOS device technology and its impact on circuit design. Dr. Loke summarized the importance of understanding the impact of effects such as halo implants, active area mechanical stress, and well implant mask proximity as well as limitations in IC manufacturing to successfully design analog circuits in deep submicron CMOS.

This set the stage for a follow-on tutorial on IC intrinsic reliability

fundamentals presented by Dr. Dennis Eaton of Agilent Technologies. In early March 2005, Dr. Rich Ruby of Agilent Technologies delivered a fascinating talk on film bulk acoustic resonators (FBARs) that have gained substantial penetration as high-Q duplexers in cell phones. In addition to explaining fundamentals and key aspects of FBAR integration, Dr. Ruby also provided a very insightful editorial on the



Technical Forum on Intel Itanium Processor at the Denver Chapter. L to R: Jeff Brisnehan (newly elected University Relations Officer), Alvin Loke (Chair), Sam Naffziger, Patrick Mahoney, Ben Patella, Jim Ignowski, Bob Barnes (Treasurer), and Tin Tin Wee (Secretary/Webmaster)

geopolitical battles and key players in the cell phone industry.

Our most recent event was a technical forum on Intel's latest Itanium processor, code-named Montecito, which drew a crowd exceeding 100. Multiple-core processors was the key theme in this year's ISSCC session on processors, and we were fortunate to have Sam Nafziger, Patrick Mahoney, Ben Patella, and Jim Ignowski of Intel, Fort Collins, present a total of four papers that were recently delivered at ISSCC in San Francisco. They shared overviews of Itanium's dual-core architecture and elucidated their clock distribution strategy, as well as their sophisticated power and thermal management control systems.

The chapter officers were also involved in community service, serving once again as science fair judges at Harris Bilingual Elementary in Fort Collins. First place went to a project that systematically investigated the effectiveness of household cleaning agents.

To establish a tighter relationship in order to sponsor activities with Colorado State University in Fort Collins, Jeff Brisnehan of Agilent Technologies was recently elected to the officers team to support University Relations.

We look forward to growing participation in upcoming seminars. Please visit our web site for more information about our chapter events including past presentation slides. ewh.ieee.org/r5/denver/sscs/

Hong Kong Chapter Events

Mansoon Chan, Hong Kong Chapter Chair, mchan@ee.ust.hk

Hong Kong Chapter hosted the Second International Workshop on Compact Modeling

Following the success of the 1st International Workshop on Compact Modeling (IWCM) held in Yokohama, Japan in 2004, the second IWCM was held in conjunction with the Asia and South Pacific Design Automation Conference (ASP-DAC) in Shanghai on January 20, 2005.

The goal of the workshops was to provide an opportunity for discussion and presentation of advances in modeling and simulation of integrated circuits. Researchers from USA, Japan, Singapore, Taiwan, Hong Kong, and China presented the most recent advances in the field of compact modeling. The Hong Kong Chapter organized the workshop while Shanghai provided the site.

Hong Kong Announces 2005 IEEE Conference on Electron Devices and Solid-State Circuits

The joint SSCS/EDS Chapter also announces their December 19-21 Conference. The EDSSC'05 Conference is a major biennial event organized by the joint Chapter in Hong Kong. A Call for Papers has been issued. For more information: www.ee.ust.hk/ieee_eds/edssc

Shanghai Chapter Hosted Asia and South Pacific DAC

Tang Ting-Ao, Shangahi Chapter Chair, tatang@fudan.edu.cn

The Shanghai Chapter organized the Tenth Asia and South Pacific Design Automation Conference (ASP-DAC 2005) during January 18-21, 2005 in Shanghai.

On the first day, 6 tutorials were given by experts and professors from NEC Labs, Philips Research Labs, IBM Research, University of Michigan, Katholieke Universiteit Leuven, University of Minnesota, University of Maryland, Fujitsu Laboratories of America, Inc., University of Tokyo, MIT and others.

- C-based design: industrial experience
- Power aware design for performance: practical techniques and tools to achieve custom-like performance in power-aware ASIC design flow
- Automated macro-modeling techniques for design of complex analog and mixed-signal integrated systems
- Intellectual property protection in semiconductor and VLSI design
- Current practices and future directions in High-Level Design

Verification

- Chip-package co-design: power integrity issues, parasitic extraction, model order reduction via parameters, and design methodology

Mr. Zhenghua Jiang from the National People's Congress of China delivered a keynote speech entitled The Development of IC Industry in China. Mr. Rajeev Madhavan from Magma Design Automation spoke in detail on the topic Silicon Compilation: The Answer to Reducing IC Development Costs, and Professor Jan M. Rabaey from U.C. Berkeley delivered a talk on Design at the End of the Silicon Roadmap.

9 Technical Sessions were carried out in 6 parallel meeting rooms on these topics: System Level Design Methodology, Embedded and Real-Time Systems, Behavioral/Logic Synthesis and Optimization, Validation and Verification for Behavioral/Logic Design, Circuit Optimization and Simulation, Physical Design and Interconnect Optimization, Test and DFT, Analog and RF Circuit Design, Design for Manufacturability and TCAD, Re Configurable Systems and Leading Edge Design.

Three Panel Discussion Sessions attracted many attendees:

- Who is Responsible for the Design for Manufacture Issues in the Era of Nano-Technologies?
- Are we ready for System-Level Synthesis?
- EDA Market in China

During the Conference, a University Design Contest was arranged, a PhD forum was also held for the first time at ASP-DAC, and a small EDA exhibition was held. Additional sponsors also scheduled satellite workshops in conjunction with ASP-DAC: the 3rd Asia University Semiconductor Design Workshop and the Compact Modeling Workshop.

NSW Australia Chapter Focused on Distributed Real-time Embedded Systems

Petru Eles of Linkoping Explains Analysis and Optimization

The SSCS New South Wales Aus-

tralia Chapter met 23 February 2005 to hear Professor Petru Eles of Linköping University, Sweden speak on the “Analysis and optimization of distributed real-time embedded systems.”

The presentation started by identifying some of the main challenges faced by designers of modern, highly complex and sophisticated embedded systems. The main focus was on time critical applications implemented as distributed systems, which are typical, for example, in the automotive area.

Efficient optimization of such systems is impossible without proper analysis, estimation methods and adequate design tools. Several new and challenging problems are due to the heterogeneous and communication intensive nature of these applications.

After introducing a system-level design flow for embedded real-time systems, Eles concentrated on the problems of timing analysis, communication synthesis, and function-

Petru Eles is Professor of Embedded Computer Systems with the Department of Computer and Information Science, Linköping University, Sweden. His current research interests include hardware/software co-design, real-time systems, design of embedded systems, electronic design automation, and design for testability. He has published a large number of technical papers in these areas and coauthored the books *System Synthesis with VHDL* (Kluwer Academic Publishers, 1997) and *System-Level Design Techniques for Energy-Efficient Embedded Systems* (Kluwer Academic Publishers, 2003). He received two best paper awards at the European Design Automation Conferences (EURO-DAC'92 and EURO-DAC'94) and a best presentation award at the 2003 IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis. Petru Eles is an Associate Editor of the IEE Proceedings - Computers and Digital Techniques, and has served on the Program Committees for numerous International Conferences, such as Design and Test in Europe (DATE), the International Conference on Computer Aided Design (ICCAD).

ality mapping. Both timing analysis and system optimization were considered in the context of complex applications consisting of both event triggered and time triggered components that communicate through static and dynamic communication protocols

The Chapter chair, Steve G. Duval of Intel, often schedules NSW chap-

ter meetings at Macquarie University. Duval has just completed his three year term as chair of this joint Circuits and Systems Society and Solid-State Circuits Society chapter. NSW Society members interested to see future professional and technical events should contact the NSW IEEE Section Chair, Graeme Gwilliam. gb.gwilliam@ieee.org •

5th International Low Power Design Contest at ISLPED

The International Symposium on Low Power Electronics and Design is holding the 5th International Low Power Design Contest in Marriott Del Mar Hotel, San Diego, California, on August 8-10, 2005 to provide a forum for universities and research organizations to showcase original “power-aware” designs and to highlight the innovations and design choices targeted at low power. The goal is to encourage and highlight design-oriented approaches to power reduction. The best designs will be selected and invited for presentation at ISLPED 2005, San Diego August 8-10, 2005.

A special session in the symposium will be devoted to the Low Power Design Contest. An industry-sponsored cash award will be awarded to each selected design entry (up to 5 entries may be selected). This could be used to defray the travel and living expenses for the speaker.

The deadline for submissions is June 13th, 2005. Entries should be submitted electronically (in PDF or Postscript format) to the Design Contest Chairs:

David Scott
Email: David.Scott@ti.com
Texas Instruments

13560 N. Central Expressway, MS3735
Dallas, Texas 75243, USA

Massoud Pedram
Email: Pedram@usc.edu
University of Southern California,
Dept. of EE-Systems, EEB-344,
3740 McClintock Ave.
Los Angeles, CA 90089-2562, USA

For more contest details see www.islped.org/Design-Contest.

The contest is sponsored by: Intel, Texas Instruments, IBM, Magma
ACM/IEEE International Symposium on Low Power Electronics and Design
Homepage: www.islped.org/ •

The Solid-State Circuits Newsletter is issued online every two months

www.ieee.org/portal/site/sscs

Subscribe at sscs.org/e-news

Congratulations New Senior Members

Claudius Dan

Veronique Ferlet-Cavrois

Tzyy-Sheng Horng

Per LP Ingelthag

Minglai Kao

Sverre U. Lidholm

Bertil C. Linder

Piero Malcovati

Monte F. Mar

Christos M A Papavassiliou

David V. Plant

Carlos E. Saavedra

Emilio A.Sovero

Lars G. Svensson

Thomas G. Swahn

Johan D. van der Tang

C. Patrick Yue.

Plan a Senior Member Nomination Night

Are you looking for a way to make Senior Member elevation easier to arrange for colleagues in your area? Plan a Senior Member Nomination Night at your local chapter. With Senior Members and Fellows willing to coach candidate Senior Members, the evening becomes a social and networking event.

First identify Senior Members and Fellows through your Section's membership database. They don't have to be SSCS members, simply IEEE members Senior grade or higher. Contact them personally to ensure their commitment to coach candidates and make this a successful event. Plenty of higher grade Members per nominee is preferred; the Central Texas Section, who has organized these

events for 3 years now, recommends 2 higher grade Members for each candidate member.

When you invite prospective Senior Members, remind them to review the requirements so they arrive prepared. They should bring their resume to help guide conversations with the higher grade members offering to provide references.

The evening of the event the Senior Members and Fellows work one on one with candidate members, clarifying the significant performance requirement of the application process. Once documented, this makes the reference writer's job much easier. When the Section takes the job of nominating the candidate, just two references instead of three are needed.

The Senior Member process is all

online now. Schedule the evening in a room with network access and a number of computers. Central Texas recommends at least a dozen computers. Their program has resulted in 75, 28 and 12 senior member applications approved over the three years with only five applications total not accepted for all three years. Have some snacks and beverages to keep the evening casual and the conversation flowing. Chatting around the tables and making careers the feature of the evening, offers the chance to exchange backgrounds and talk about useful career directions.

Read about Central Texas Section Senior Member campaign, an online case study which describes their highly successful process.

www.ieee.org/seniormember ●

March e-News Features

Beginning 2005, the SSCS newsletter is bimonthly, with issues printed just three times a year. Since the January print issue, SSCS has issued a March e-news sent by email, that covered these topics.

- 14 New IEEE Fellows from SSCS in the class of 2005
- The new SSCS Digital Archive available in February that adds CICC and for the first time ESSCIRC.
- An obituary of Don O. Pederson, a CAD Pioneer and co-founder of the Solid-State Circuits Council.
- The announcement of the 2003 JSSC Best Paper Award for "Second-order intermodulation mechanisms in CMOS downconverters" by Danilo Manstretta, Massimo Brandolini and Francesco Svelto.
- Highlights of the February AdCom Meeting and Chapters Meeting
- A Call for Nominees for the SSCS Administrative Committee for which the deadline passed on May 1.
- News about the RFIC Symposium in June.
- The list of top selling books from major technical publishers at ISSCC.

To review issues online select e-news Archive from the home page of the SSCS-e-news.

www.ieee.org/portal/site/sscs

To receive the SSCS July e-news which will not be available in print, please request to join the list at www.ieee.org/ra/e-notice/sscs-notice.html ●

The screenshot shows the SSCS website interface. At the top, there is a navigation bar with links for Home, Search IEEE, About, Web Account, and Contact IEEE. Below this is a banner for the SSCS 40th Anniversary. The main content area is titled "featured in this issue" and highlights the "MARCH 2005 ISSUE". Key features listed include:

- Featured:** SSCS 1998 Fellows for the Class of 2005. A new group of 14 SSCS members have been named IEEE Fellows for the class of 2005. They are including: (left to right) Tom Dick, Lawrence W. Hooper, Robert Hays, David John Cuman, Arnold Andrew Chalmers, Brian McDermid, Michael H. Hoyle, Daniel Lavanon, Liang Hsuan-Ming, Karlberg, Margaret, Penman, O. Ananda Mohan, Shih-Shyan and Jason Chih-Shan Wu.
- Network From SSCS:** 2004 SSCS Digital Archive DVD Issued. A new version of the SSCS Digital Archive was issued in November 2004. The set of DVDs includes all the articles of the IEEE Journal of Solid State Circuits from the first issue through 2004, plus complete digital files from two conferences. These conferences digital collections are complete from the archive through 2004: ISSCC, Custom Integrated Circuits Conference and the Symposium on VLSI Circuits. The fourth conference digital of the European Solid State Circuits Conference from 1987 through 2004 are collected here for the first time. You can order it directly from the IEEE Store.
- Obituary:** Donald O. Pederson, CAD Pioneer and SSCS Founder, Dies at 79. Professor Donald O. Pederson, a pioneering engineer whose insight and leadership were instrumental in shaping the semiconductor industry, passed away on Christmas Day 2004 after a long illness. Due to winter

SSCS IEEE Fellows for the Class of 2005

An IEEE Fellow holds the highest grade of IEEE membership. Elevation to Fellow recognizes unusual distinction in the profession, and is conferred by the IEEE Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest. The accomplishments honored contribute significantly to the advancement of engineering, science, and technology.

After a rigorous evaluation process performed each year by the IEEE Fellow Committee, a slate of candidates is proposed to the IEEE Board of Directors for approval. The number of successful candidates in any year must not exceed one-tenth of one percent of IEEE members. For 2005, of the 268 Fellows elevated, the following four were evaluated by the Solid-State Circuits Society. The additional 10 Fellows are SSCS members who have been elevated by other Societies.

Prof. Terri S. Fiez

Oregon State University, Corvallis, OR, USA

for contributions to analog and mixed-signal integrated circuits



Terri S. Fiez received the B.S. and M.S. in Electrical Engineering in 1984 and 1985, respectively, from the University of Idaho, Moscow. In 1990, she received the Ph.D. degree in Electrical and Computer Engineering from Oregon State University, Corvallis. From 1985 to 1987 and in 1988 she worked at Hewlett-Packard Corp. in Boise and Corvallis, respectively.

In 1990, Dr. Fiez joined Washington State University as an assistant professor where she became an associate professor in 1996. In the fall of 1999, Prof. Fiez joined the Department of Electrical and Computer Engineering at Oregon State University as Professor and department head. She became Director of

the School of Electrical Engineering and Computer Science in 2003. She has been involved in a variety of IEEE activities including serving on the committees for the IEEE International Solid-State Circuits Conference, IEEE Custom Integrated Circuits Conference, ISCAS, and as a guest editor of the Journal of Solid-State Circuits. Dr. Fiez was awarded the NSF Young Investigator Award and the Solid-State Circuit Predoctoral Fellowship. Her research interests are in the design of high performance analog signal processing building blocks, simulation and modeling of substrate coupling effects in mixed-signal ICs, and innovative engineering education approaches.

Dr. Koichiro Ishibashi

Semiconductor Technology Academic Research Center (STARC)
Yokohama, Japan

for technical contributions to developments of low-power SRAMs and MCUs



Koichiro Ishibashi received the B.E. degree from Sophia University, Tokyo, Japan in 1980, M.S., and Ph.D. degrees from the Tokyo Institute of Technology, Tokyo, Japan, in 1982 and 1985, respectively. In 1985, he joined Central Research Laboratory, Hitachi, Ltd., where he was involved in research and development of high density SRAMs, low-power RISC microprocessors, and low-power CMOS circuit technology. He led the Low Power Technology Group of Semiconductor Technology Academic Research Center (STARC) from 2001 to 2004. Since 2004, he has been the senior manager of Advanced Design Framework Development Department of Renesas Technology Corporation.

During his research career, he has presented more than 80 papers and presentations as an author or co-author, mainly on high density

SRAMs and circuits for low power MCUs in the Journal of Solid-State Circuits, ISSCC, the Symposium on VLSI Circuits and others. He holds 72 patents granted in the U.S. and Japan. He has made contributions to the IEEE Solid-State Circuits Society as a member of program committees, a session chair/co-chair of ISSCC, a rump session organizer and a panelist, a short course organizer and a lecturer at VLSI Symposia. He contributed to the IEICE (Japan) as a guest editor or an associate editor for a number of IEICE transactions. He received an R&D 100 award for the Development of SH-4(SH7750) Series Microprocessor in 1999, and the Takeda Techno-Entrepreneurship Award for Low Power Circuit Technology of Microcontrollers in 2001(Japan).

Dr. Laurence W. Nagel

Omega Enterprises, Randolph, NJ, USA

for contributions to the field of integrated circuit simulation



Laurence W. Nagel has worked in the integrated circuit industry for about 30 years. While earning his B.S., M.S., and Ph.D. degrees at the University of California, he developed the SPICE circuit simulation program and launched a cottage industry of SPICE simulation tools. Mr. Nagel then began a 20 year career at Bell Laboratories which included developing the ADVISE circuit simulation program, participating in the development of process and device simulation tools, participating in the development of the Kull-Nagel bipolar model; designing analog circuits for submicron NMOS processes, working in the AT&T Intellectual Property Division working on assertion of patents and negotiation of patent licenses, and serving as project manager in the development of the Celerity circuit simulation pro-

gram. Mr. Nagel joined Anadigics, Inc. in 1995, where he worked on supporting simulation of RF integrated circuits; modeling and characterization of GaAs MESFET device processes; and importing silicon CMOS design tools and foundry support. In 1998, Mr. Nagel founded his own company, Omega Enterprises, which offers consulting services in analog and RF integrated circuit design, device modeling, circuit simulation, and expert witness work in patent and trade secret litigation.

Dr. Kazuo Yano

Central Research Laboratory, Hitachi, Limited Tokyo Japan
for contributions to nanostructured-silicon devices and circuits and advanced CMOS logic



Kazuo Yano was born in Sakata in Japan on October 18, 1959. He received the B.S., M.S., and Ph.D degrees from Waseda University,

Japan, in 1982, 1984, 1993, respectively. He joined the Central Research Laboratory, Hitachi Ltd. in 1984. He has been interested in the limitations of LSIs and breakthrough technologies. He studied MOS/bipolar devices for low-temperature computers, CMOS/BiCMOS logic circuits, and single-electron devices and system-LSI design methodology/tools. From 1991 to 1992 he was a Visiting Scientist at the Arizona State University, working on single-electron transport physics with Professor D. K. Ferry. He conceived complementary pass-transistor logic (CPL), and also did pioneering work on the synthesis of pass-transis-

tor logic circuits (LEAP) and world's first room-temperature single-electron memories. He supervised research teams of SuperH mobile application processors, which are now widely used for camera phones, low-power circuit design, DRAM, flash memory, logic-optimization tools, design for test and flexible computing engine. Since April 2004, he has been the Project Leader of the Sensor Net Strategic Project at the Central Research Laboratory and also the Laboratory Manager of the Human Intelligence Laboratory at the Advanced Research Laboratory. He is supervising research teams focused on sensor net, ultra-wideband wireless technology, advanced human-machine interaction, computer vision, and quantum information technology.

He is a member of the IEEE, the Japan Society of Applied Physics, and the IEICE of Japan. He received 1994 IEEE Paul Rappaport Award, 1996 IEEE Lewis Winner Award and 1998 IEEE Jack Raper Award. He was a solid-state device subcommittee member of IEDM and a panel committee member of Design Automation Conference.

Additional SCS Members Recognized As IEEE Fellows

Prof. David John Comer

Brigham Young University
for leadership in engineering education and publication of electronic circuit design textbooks

Prof. Janusz Andrzej Dobrowolski

Warsaw University of Technology
for contributions to computer-aided design of microwave networks

Prof. Ken-ya Hashimoto

Chiba University
for contributions to simulation and design for surface acoustic wave devices.

Prof. Michael N. Huhns

University of South Carolina
for contributions to artificial intelligence applications in distributed computational environments.

Prof. Domine Leenaerts

Philips Research Laboratories
for contributions to artificial intelligence applications in distributed computational environments

Prof. Lloyd Wilson Massengill

Vanderbilt University
for contributions to radiation effects in microelectronics

Prof. Kartikeya Mayaram

Oregon State University
for contributions to coupled device and circuit simulation

Dr. Pemmaraju V. Ananda Mohan

Electronics Corporation of India Limited
for contributions to telecommunications technologies

Dr. Shinji Okazaki

Association of Super-Advanced Electronics Technologies
for contributions to the resolution enhancement technology in optical and electron-beam lithography

Prof. Jason Chik-Shun Woo

UCLA
for contributions to nanoscale silicon on insulator and bulk metal oxide semiconductor device physics and technology •

IEEE Virtual Museum Launches Exhibit on Electronic Instruments

23 March -- The IEEE Virtual Museum has launched its latest exhibit, "Songs in the Key of E," which explores the numerous ways electronics have been used to create music. With examples such as the singing arc, the theremin and the synthesizer, among

others, the exhibit highlights both the inventors of electronic instruments and the instruments themselves, and uses audio clips to demonstrate the various sounds.

This is the eighth IEEE Virtual Museum exhibit since its launch in

2002. Aimed at pre-college students and their educators, the museum explores the global impact of electrical and information sciences and technologies to demonstrate how relevant engineers are to society.

www.ieee-virtual-museum.org/ •

Wireless Wednesday at DAC

Why would a designer for a wireless system attend DAC? Who are the designers for a wireless system anyway?

Ingrid Verbauwheide, Design community chair of the 42nd DAC, ingrid@ee.ucla.edu

A complete wireless system is a very complex design problem. It requires designers from very different backgrounds. The communication engineer needs to figure out the wireless system performance, and will run lots of simulations in Matlab or Simulink to get the bit error rate (BER) that he or she needs. The team will also need a MAC designer who is willing to dig into the standards and implement the MAC protocols with minimum resources and within the latency and throughput requirements. The hardware or digital designer will develop the building blocks to implement the next generation LDPC coder or Turbo accelerator. The analog and RF designers are probably in a different department worrying about getting the power amplifiers, LNAs, D/As and A/Ds operating at 1V and with a minimal power budget. Then there is the poor system designer that needs to figure out how all the modules communicate, can be integrated and tested.

The wireless day at DAC aims at bringing designers of wireless systems together with design tools and methods providers.

It includes a panel Wireless Platforms: GOPS for Cents and Milli-



Watts with speakers from small and large design houses. They will discuss the opportunities offered by truly ubiquitous connectivity: it is leading to revolutionary changes in the way computer, communication, and consumer systems operate and interact. Panelists will debate the various wireless implementation platforms that are breaking new ground, examining issues of efficiency, flexibility and programming models.

The special session on emerging directions in wireless identifies some major new trends and technologies in wireless and the impact those

would have on implementation strategies, architectures, and methodologies. It includes presentations on cognitive radio techniques, MIMO technologies and RF-MEMs. In the Best of ISSCC session, the presenters will focus on the design methods behind some of the most advanced IC designs presented at ISSCC in February 2005. A design methods session gives typical examples of design technology focused especially at wireless problems.

The DAC exhibit floor will also have a special emphasis on wireless including interviews with Gadi Singer from Intel and Mike Muller from ARM.

There will be a showcase of wireless products and a “wireless walk” highlighting CAD companies with tools targeted to wireless applications.

Of course DAC offers many more sessions on topics of interest to designers, including sessions on design for manufacturing, embedded systems, verification, design for deep submicron, and so on.

The 42nd Design Automation Conference will run in Anaheim from June 13 to 17, 2005.

The Wireless Wednesday is June 15.

The conference URL is

www.dac.com

SSCS EVENTS CALENDAR

Also posted on www.sscs.org/meetings

SSCS SPONSORED MEETINGS

2005 Symposium on VLSI Circuits

www.vlssymposium.org

16–18 June 2005

Kyoto, Japan

Paper deadline: passed

Contact: Phyllis Mahoney,

vlsvl@vlssymposium.org

or Business Center for Academic Societies, Japan,

vlssymp@bcasj.or.jp

2005 CICC Custom Integrated Circuits Conference

www.ieee-cicc.org

18–21 September 2005

San Jose, CA, USA

Paper deadline: passed

Contact: Ms. Melissa Widerkehr,

cicc@bis.com

2005 A-SSCC Asia Solid-State Circuits Conference (the first meeting)

www.a-sscc.org/

1–3 November 2005

Hsinchu, Taiwan

Paper deadline: 3 Jun 2005

Contact: org@a-sscc.ee.ntu.edu.tw

2006 ISSCC International Solid-State Circuits Conference

www.isscc.org

5–9 February 2006

San Francisco Marriott Hotel,

San Francisco, CA, USA

Paper deadline: 19 September 2005

Contact: Courtesy Associates,

ISSCC@courtesyassoc.com

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2005 International Conference on VLSI Design

www.isical.ac.in/~vlsi2005

3–7 June 2005

Taj Bengal, Kolkata, India

Paper deadline: passed

2005 Radio Frequency Integrated Circuits Symposium

www.rfic2005.org

12–14 June 2005

Long Beach, CA, USA

Paper deadline: passed

2005 Design Automation Conference

www.dac.com

13–17 June 2005

Anaheim, CA, USA

Paper deadline: passed

2005 Symposium on VLSI Technology

www.vlssymposium.org

14–16 June 2005

Kyoto, Japan

Paper deadline: passed

2005 European Solid-State Circuits Conference

www.esscirc2005.org/

12–16 September 2005

Grenoble, France

Paper deadline: passed

2005 Bipolar/BiCMOS Circuits and Technology Meeting

www.macs.ece.mcgill.ca/~rfic/bctm05/index.htm

9–11 Oct 2005

Santa Barbara, CA

Paper deadline: passed

2005 Compound Semiconductor IC Conference

www.csics.org/

29 Sep–1 Oct 2005

Palm Spring, CA

Paper deadline: 9 May 2005

2005 International Conference on Computer Aided Design

www.iccad.org

6–10 November 2005

San Jose, CA, USA

Paper deadline: passed

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