Announcing a Special Section in IEEE Access:
System-Level Design Automation Methods for Multi-Processor System-on-Chips

Submission Deadline: November 15, 2016

IEEE Access invites manuscript submissions in the area of System-Level Design Automation Methods for Multi-Processor System-on-Chips

With the advent of new device technologies, the feature size of transistors decreases and the transistor count increases exponentially. This also leads to the explosive growth in computation power and functionalities available on a single chip. In recent years, System-on-Chips (SoCs), in which all the functionalities of a system are integrated in a chip, have entered to the multi-core era due to the increasing number of services provided by a system. However, this also increases the complexity of designing such chips which have grown at a very fast pace.

To reduce time-to-market of SoCs, Electronic Design Automation (EDA) tools have been utilized to enable efficient design space exploration, verification and simulation. However, with the advent of MPSoCs (Multi-Processor System-on-Chips), conventional EDA tools that utilize RTL (Register-Transfer Level) abstraction as the highest abstraction level have been shown not able to cope with the growth of the chip complexity of modern designs. Therefore, electronic system-level (ESL) design, which has abstraction level higher than RTL, has been proposed as the solution for minimizing the gap between chip complexity and design productivity in the multi-core, even many-core, era. System-level synthesis automatically implements the hardware and software systems of the target system based on the application models that represent the behavior of the application set running on the system. The hardware and software components considered by system-level synthesis are hardware modules like IP cores and memory modules and software kernel functions, which are coarser grained compared to RTL or gate-level synthesis. The synthesis results of system-level tools are then passed to lower level synthesis tools for further refinement. Therefore, the robustness and effectiveness of system-level synthesis technology is crucial to the design of an MPSoC.

To facilitate a good system-level design, the system-level synthesis tools should consider major design issues at the early design stage. For modern chip designs, the major design issues include power consumption, and thermal and variation problems. Moreover, several emerging technologies and novel architecture have been proposed for MPSoC designs, such as the 3D die-stacking technology that is enabled by Through Silicon Vias (TSVs), and Single-ISA (Instruction Set Architecture) heterogeneous multi-core architecture. These emerging technologies also have their own design issues should be addressed during chip design. Therefore, in addition to performance and cost issues, these issues should also be addressed at early design stage by the system-level synthesis tools to achieve a good whole system design.

System-level synthesis tools usually implement one or more of the following synthesis steps, resource allocation, resource binding or application mapping, and scheduling. Resource allocation decides which
hardware modules, e.g. processing elements (PEs) and memory modules, should be allocated in the target system. Resource binding performs the mapping between tasks/data and processing/memory modules. A task indicates a kernel function of the application running in the system. When multiple tasks or data accesses may compete for the same resource, scheduling is performed to prioritize the tasks or data accesses executed on the resource. The aforementioned design issues can be considered alone with any of the synthesis steps.

Therefore, the purpose of this Special Section in IEEE Access is to call for papers related to research in novel system-level synthesis tool designs concerning issues related to emerging technologies and design issues.

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