

IEEE Santa Clara Valley Solid State Circuits Chapter
<http://www.ewh.ieee.org/r6/scv/ssc/index.html>

Introduction to Analog IC Design

Instructor: Ahmad Baghai Dowlatabadi, P.E., Ph.D.

Date: : Aug. 18th - 29th, 2003, Mon. Wed. & Fri. (for 6 days total) 8-12 noon.

Place: Cogswell College

Overview - The course introduces the principles of analog IC design in CMOS, BJT and BiCMOS technologies. Yet, emphasis would be placed on circuits in CMOS process. Small-signal and large-signal analysis of basic CMOS analog circuits are covered to build a foundation for more complicated and advanced designs. The course is structured for those who are interested in starting a career in analog IC design area. Hence, it covers the basics of issues related to fundamental analysis (i.e. "paper design"). Use of any design software is not needed and is not covered. The goal is to provide a strong analysis scheme so it can be used in future design activities.

Intended Audience The course is intended for practicing Engineers who are unfamiliar with basic issues and challenges in analog IC design area, or are working as design Engineers and simply would like to review all of the basics.

Prerequisites - A BSEE (or equivalent) with knowledge of linear circuit analysis (i.e. KVL, KCL, frequency and voltage gain & phase analysis) along with clear understanding of device physics and elementary control theory.

Course Outline - Topics that would be covered are:

- Small-and large-signal models for BJT transistors that are used in analog design are described.
- Small-and large-signal models for MOS devices used in typical analog design.
- Analysis of basic analog circuits such as current source/sink, inverters, cascade amplifiers, differential amplifiers, output stages and switches are described.
- Fundamentals of frequency and time domain analysis are described for all of the blocks.
- Issues related to stability (gain & phase in frequency and time domain) for each block is covered.
- After covering basic blocks, design of more complicated cells such as amplifiers, comparators and bandgap voltage references are described.

Instructional Method - Daily lecture will be given in class with limited number of handouts from IEEE journals and conferences for additional readings. Furthermore, homework problems along with simple design projects (which DO NOT require the use of any design software) will be assigned for practice.

Text book is "CMOS Analog Circuit Design", Oxford University Press (**a copy is provided and is included in the fee**).

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Fee Structure: - The fee for the course along with a copy of text book is structured as;

<i>Attendees</i>	<i>IEEE Members</i>	<i>Non-Members</i>
Employed	\$135	\$160
“On Forceful Job Transition” (aka unemployed)	\$60	\$65
Students (valid ID needed)	\$60	\$65

Please complete the form below and submit it along with a check made to:
IEEE SSC (of SCV)
and mail them both to:

Mr. Jai Subrahmanyam
3480 Granada Avenue, Apt 111
Santa Clara, CA 95051

Please NOTE: The deadline for registration is Aug. 2nd, 2003 in order to receive the books on time for the class. **Thus, registration check must be in our possession by Aug. 2nd, 2003.**

Name: _____ IEEE Member No: _____

Address: _____

Employed By: _____

Student at (include ID No.): _____

Email Address: _____

Day Time Phone: _____ Evening Time Phone: _____